EAI®

680

SCIENTIFIC COMPUTING SYSTEM

REFERENCE HANDBOOK

22-3-95

EAI 680

SCIENTIFIC COMPUTING SYSTEM

REFERENCE HANDBOOK

 • PRINTED IN U.S.A. • PUBL. NO. 00 800.2048-0 • OCTOBER 1966

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Printed in U.S.A.

Bulletin No. IL-64104-6
June, 1966

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CHAPTER 1

INTRODUCTION

1.1 PURPOSE OF THIS MANUAL

This manual is intended to fill two specific needs: The need for a text for the programmer to study to familiarize himself with the computer, and the need for a reference book for the experienced programmer to look up an occasional circuit. To accomplish these goals, the main body of the book (Chapters 1 through 21) is written in "textbook" format, covering each component in turn. The reader interested in rapidly learning how to use a given component should read only the initial paragraphs of each chapter, and skip the paragraphs marked "Circuit Details", which contain schematics, block diagrams, and other information on the internal hardware.

Explicit patching diagrams and suggested programmer's symbols for analog components are given in Appendix 1, which is organized somewhat differently from the rest of the book. The rest of the book is organized by *components;* Appendix 1 is organized by *applications*.

1.2 BACKGROUND KNOWLEDGE ASSUMED

This handbook is intended to provide the experienced analog programmer with a description of the specific features in the 680. Familiarity with analog computation *in general* is assumed. Hence, no information on programming and scaling is included, with one principal exception. This exception is Appendix 4, which covers the log/exponential DFG, and includes a considerable amount of scaling detail, since most textbooks on analog computation do not cover log/exponential scaling adequately.

1.3 STRUCTURE OF THIS MANUAL

The manual may be divided into three main subdivisions, exclusive of appendices:

1.3.1 Chapters 2 through 5

These chapters contain basic programming and operating information for the computer as a whole.

1.3.2 Chapters 6 through 18

These chapters contain descriptions of individual components. Each chapter covers a single component or a group of closely related components.

1.3.3 Chapters 19 through 21

These chapters contain information on mode control and time scale selection. This information is not necessary for simple, straightforward problems, but can be quite useful for repetitive and iterative operation. In particular, Paragraph 20.3 contains descriptions of a number of mode control and overload detection features which are occasionally useful.

1.4 WHAT TO READ FIRST

1.4.1 Basic Information

For the reader who is just starting out, and wants to "get on the computer" for a simple problem, the following reading is recommended:

1.4.1.1 *Read Chapters 2 through 5.* These paragraphs contain basic material on "where to find things", and how to set up the problem.

1.4.1.2 Read Appendix 6, which explains the use of normally-closed patch panel contacts. These contacts appear in many schematics throughout the manual, and are essential to understanding many of the patching features. Even the reader who is not "schematic-oriented", but simply wants to know how to patch the components, should examine this appendix, and Figure 8.2. Proper use of the normally-connected pot feature can result in considerable patching simplification. Similarly, a full understanding of the Junction Inverter (Figure 9.3) requires a knowledge of how the normally-connected feedback resistor operates.

1.4.1.3 Read the paragraphs in Appendix 1 which correspond to the applications you require for the particular problem, and read the initial sections of the corresponding chapters. Refer to the photograph of the patch panel in Appendix 7.

1.4.1.4 Read Appendix 3 (Startup Procedure).

1.4.2 Further Information

Once the programmer has obtained a basic understanding of the machine and has run one or two problems, a reading of Chapters 19 through 21 is recommended, especially Paragraphs 20.1, 20.2, and 20.3. All appendices should be read, or at least skimmed, with the possible exception of Appendix 4 (if the programmer has no interest in logs or exponentials).

The balance of the book may be read at the programmer's discretion. In particular, the paragraphs marked "Circuit Details" may be of great interest to some programmers and of little or no interest to others.

CHAPTER 2

GENERAL MACHINE ORGANIZATION

An overall view of the 680 Console is given in Figure 2.1. The major portions of the console are briefly described in this chapter. More detailed information is given in subsequent chapters.

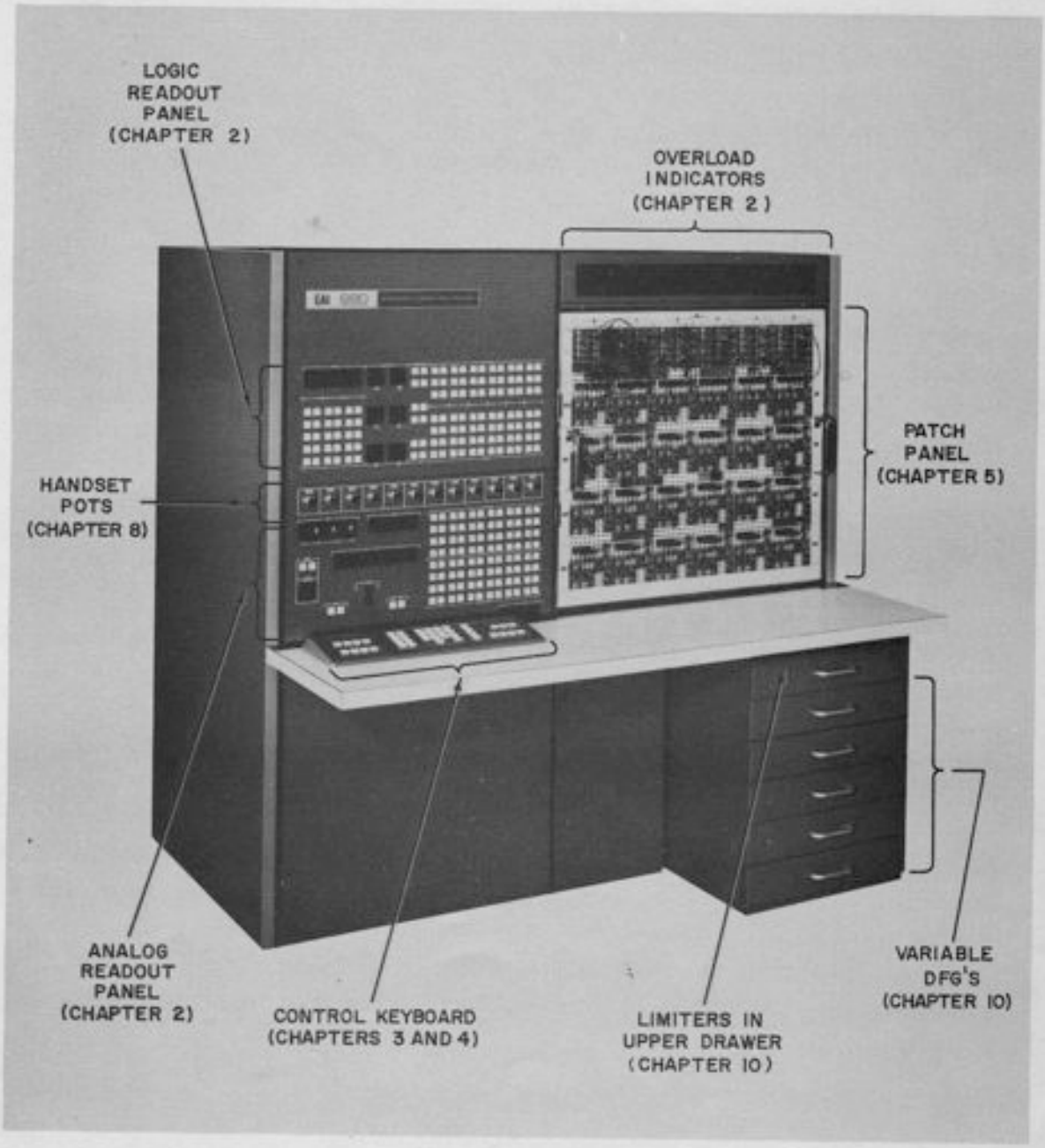


Figure 2.1. Overall View of the 680

2.1 THE PATCH PANEL

The patch panel is divided into five rows. The upper row is devoted to logic elements (flip-flops, counters, gates, etc.). The lower four rows contain the analog elements. Almost all computing components are housed in slideout trays directly behind the panel. Further information on the patch panel organization is given in Chapter 5.

The panel is of aluminum, and has a total of 4080 holes. A motorized drive is provided for insertion and removal. See Appendix 3 for the procedure.

2.2 THE OVERLOAD INDICATORS

Directly above the patch panel are the overload indicators (Figure 2.1). When a component overloads, the appropriate light on the overload panel glows. Note that the overload indicators for the amplifiers are laid out in four rows, similar to the layout of the patch panel itself. The first two digits are common to a block of ten amplifiers, and only the last digit lights up. A similar arrangement is used for the VDFG's and multipliers.

2.2.1 Overload Criteria

An amplifier is regarded as overloaded when its summing junction departs from virtual ground. This usually means that the output has been driven beyond its normal operating range. Most amplifiers are capable of producing outputs up to about 1.2 or 1.3 units (12 or 13 volts) before overloading. A VDFG is regarded as overloaded for the purpose of triggering the alarm when its output exceeds 1.05 units (10.5 volts) in magnitude. A multiplier is regarded as overloaded when the sum of the absolute values of the inputs exceeds 2.05 units (20.5 volts). Note that for this to happen, it is necessary, but not sufficient, that at least one input be greater than 1.0 unit. Under some conditions, an input greater than reference voltage can be multiplied by a smaller input correctly. For example, if X = 1.25 units (12.5 volts) and Y = 0.6 unit (6.0 volts), then $|X| + |Y| < 2.05$. The multiplier will not indicate an overload, and the output product will be correct (±0.75 unit, or ±7.5 volts). Thus the overload system is designed to respond only to genuine overloads.

Overload indication is also provided for the ±REFERENCE power supplies. A malfunction or excessive loading (such as accidentally patching reference to ground) causes an overload indication.

2.2.2 Audible Overload Alarm

In addition to the visual indication, an audible alarm is provided to which produces a tone whenever *any* component overloads. A volume control is provided for this alarm behind the logic readout panel. The volume may be varied continuously from an inaudible level up to one so loud that it may be easily heard in a room full of people and machinery.

2.2.3 Logic Level and Control

In addition to the visual and audible alarms there is an output on the logic panel which comes high whenever *any* component overloads. A stored overload feature is also provided, under logical control. For details on these features, see Paragraph 19.3.7.

2.3 THE LOGIC READOUT PANEL (Figure 2.2)

This panel contains indicators that show the state of each logic element. When the element is in the ONE state, the corresponding indicator is lit. Most of those indicators are pushbuttons as well, allowing the logic element to be set or reset manually. A listing of the indicators and controls is given below. More detailed information is given in the chapters on the individual components.

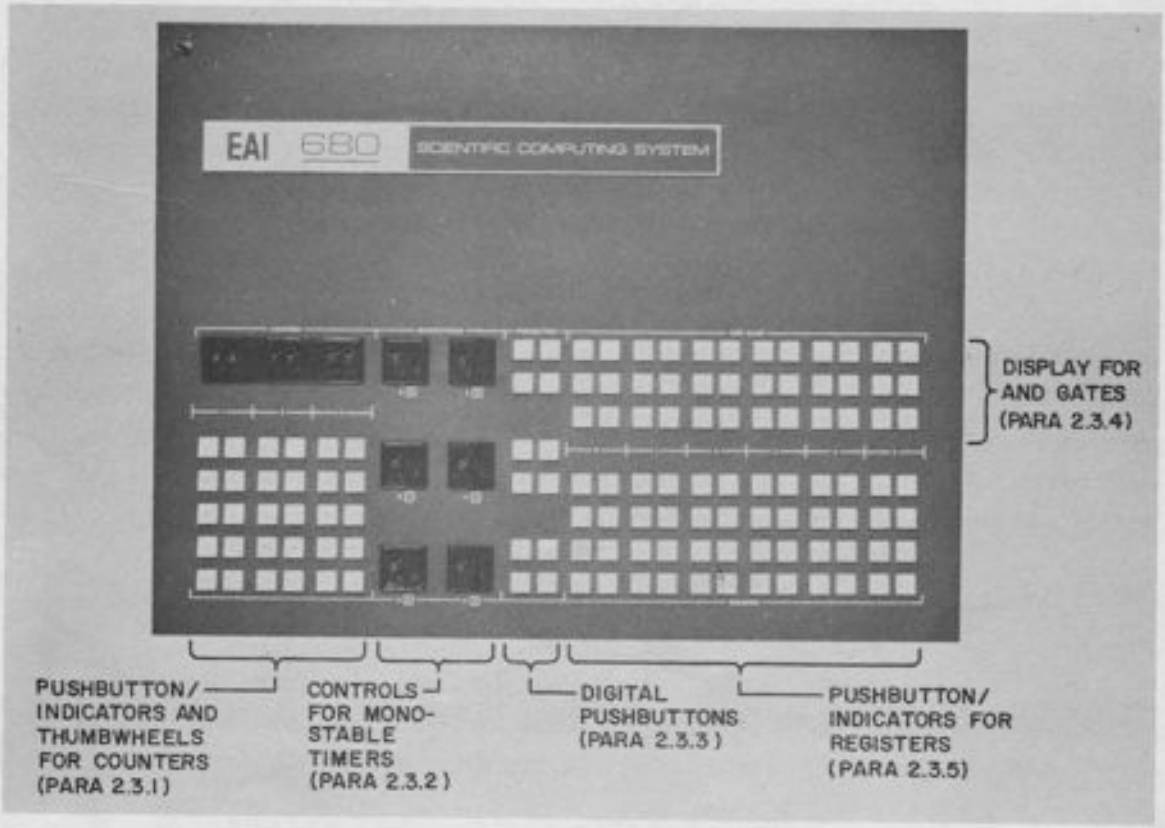


Figure 2.2. The Logic Readout Panel

2.3.1 The Counters (See Chapter 16)

Controls are provided for three BCD counters, each with two decades. The eight flip-flops in each counter are individually displayed so that the contents of the counter may be determined at any time by adding the numbers on all indicators that are lit. The indicators are also push-buttons which may be used to manually set any given flip-flop. Pushbuttons at the bottom of each column allow manual clearing. At the top of the panel, a pair of thumbwheels is provided, to allow an initial value to be loaded into the counter.

2.3.2 The Monostable Timers (See also Chapter 17)

A thumbwheel and vernier pot, used for setting the time interval, are provided for each of the six monostable timers.

2.3.3 Digital Pushbuttons (See also Chapter 18)

Six general purpose pushbuttons are provided. Each button provides a ZERO or a ONE at an output terminal on the patch panel. Each output corresponds to a pair of buttons. Depressing the button on the left sets the output to ONE; depressing the button on the right sets the output to ZERO. The button on the left acts as an indicator; it is lit when the output is set to ONE. This output is not synchronized with the system clock. When the output is set to ZERO, a synchronized blip (a pulse one clock period in length) is generated at the output terminal each time the button on the right is depressed. The complementary output is also terminated.

2.3.4 The AND Gates (See also Chapter 14)

Each AND gate in the computer is provided with an indicator which lights when the gate output is logic ONE. Each indicator is also a pushbutton. Depressing the button *has no effect* on the gate output. Since the gate is not a "memory" device, it is not possible to "SET" or "RESET" it. However, depressing the button will light the light as long as the button is held down. This feature provides a quick check for a burned-out bulb.

2.3.5 The Registers (See also Chapter 15)

Each GPR (General-Purpose-Register) contains four flip-flops. For each flip-flop, there is a pair of pushbuttons. The button on the left serves as an indicator; it lights when the flip-flop is set. It may also be used for manual control; depressing it sets the flip-flop. Depressing the button on the right resets the flip-flop.

2.4 THE HANDSET POT STRIP (Figure 2.3)

This strip contains the twelve handset pots. They are ten-turn, 5K pots, with locking knobs. See Paragraph 8.2 for further details.

2.5 THE ANALOG READOUT PANEL (Figure 2.3)

This panel contains the DVM display, display for comparators and function relays, and other controls.

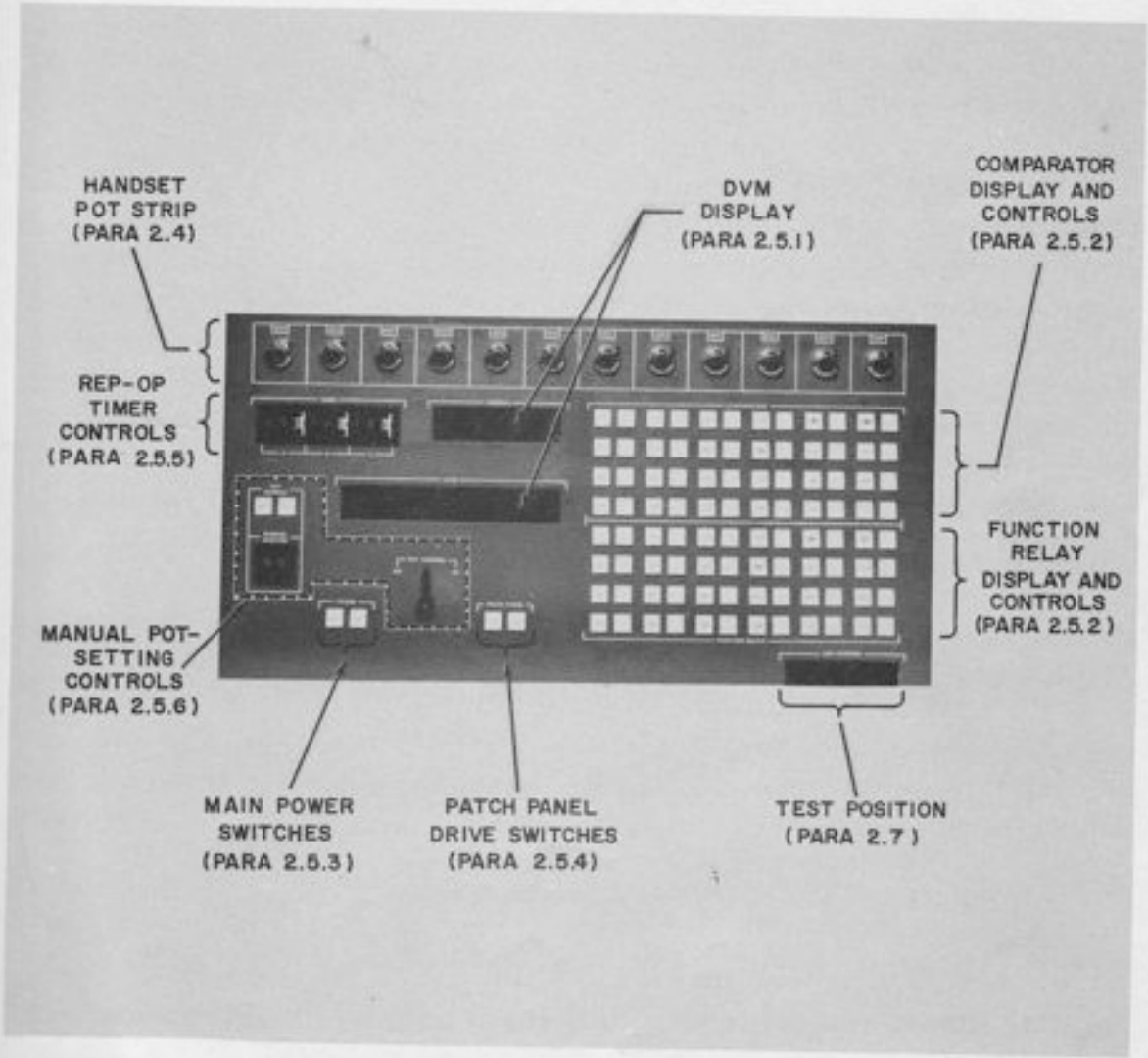


Figure 2.3. The Analog Readout Panel

2.5.1 The DVM Display

This displays the address (e.g., A25) and value (e.g., +.5942) of whatever component is addressed on the signal selector. (See Chapter 3 for a description of the signal selector.) Values are displayed on a unit-scaled basis; that is, reference voltage is taken as the unit of measurement. Hence, plus Reference is displayed as +1.0000 unit. A ±20% overrange is provided; i.e., the DVM will measure values up to ±1.1999 units (±11.999 volts).

2.5.2 The Comparators and Function Relays (See also Chapter 13)

A pair of buttons is provided for each of the 24 comparators in the computer. The button on the left is an indicator; it lights when the comparator output is ONE. Depressing this button will set the output flip-flop, forcing the comparator output on the patch panel to ONE regardless of the state of the analog inputs. Similarly, depressing the other button forces the output to ZERO. When the finger is removed from the button, the comparator reverts to normal operation, following its analog inputs. Of course, if the LATCH input is high, or the clock is in the STOP mode, the analog inputs have no effect (see Paragraph 13.2) and the comparator output remains in the state to which it was manually set. This feature is useful for checkout, since it allows the establishment of test signals at the comparator outputs.

A similar arrangement is provided for each of the 24 function relays. When a relay is in the "+" state, the button on the left is lit. This button, when depressed, forces the relay into the "+" state independently of the patched logic inputs. The button on the right, when depressed, forces the relay into the "-" state. These relays are driven by flip-flops, so that if no logic signal is patched in, they remain in the state into which they are manually set. Hence, if no logic inputs are patched, the relays may be used as manual function switches.

2.5.3 Main Power Switches

These switches apply power to the computer. Depressing the ON button turns the computer on; the OFF button turns it off. For startup procedures, see Appendix 4.

2.5.4 Patch Panel Drive Switches

These switches, marked ENG and DIS are for insertion and removal of the motor-driven patch panel. See Appendix 4 for procedure.

2.5.5 Rep-Op Timer Controls

These controls determine the duration of the computing intervals in the *Rep-op* mode. See Chapter 20, Paragraph 20.2 and 20.3 for details.

2.5.6 The Manual Pot Setting Controls

In the lower left-hand corner of the panel are a pair of pushbuttons marked POT ADDRESS and a set of thumbwheels marked MANUAL SELECTOR. Below the DVM is a lever marked POT CONTROL. These controls allow manual setting of the servo-set pots. Details are given in Chapter 4. For normal servo-setting operation, the POT ADDRESS should be in the KEYBOARD mode.

2.6 THE CONTROL KEYBOARD (Figure 2.4)

The Control Keyboard located on the shelf below the analog readout panel. Its main functions are mode control, signal selection, and pot-setting. From left to right, the buttons are as follows:

2.6.1 Logic Mode Control and Clock Rate Selection

The four buttons marked ST, 10, 10^5, and 10^6 select the clock rate for the synchronized logic elements. They form a mutually-exclusive group. (Only one of the four is lit at a time. Depressing one button lights it and extinguishes the others.) The button that is lit determines the clock rate. The "normal" rate is 10^6 pulses per second (one clock pulse every micro-second). Clock rates of 10^5 and 10 pulses per second are also provided.

NOTE

The 10^5 and 10 pulse/second clocks are only available when the rep-op timer is running.

The ST (STEP) button inhibits all clock pulses when initially depressed, and subsequently provides one clock pulse every time it is depressed. This feature is useful for problem checkout.

Below the clock rate controls is the Digital Mode Control group, another group of four mutually-exclusive buttons. The buttons marked C, S, and R put the logic into the CLEAR, STOP, and RUN modes respectively. In the CLEAR mode, all flip-flops are cleared (reset to ZERO) and

the system clock is stopped. In the STOP mode, the clock is stopped. In the RUN mode, the system clock is running at a frequency determined by the Clock Rate group of buttons mentioned above.

NOTE

The Clock Rate buttons have no effect unless the logic system is in the RUN mode. In particular, the STEP pushbutton works only in the RUN mode.

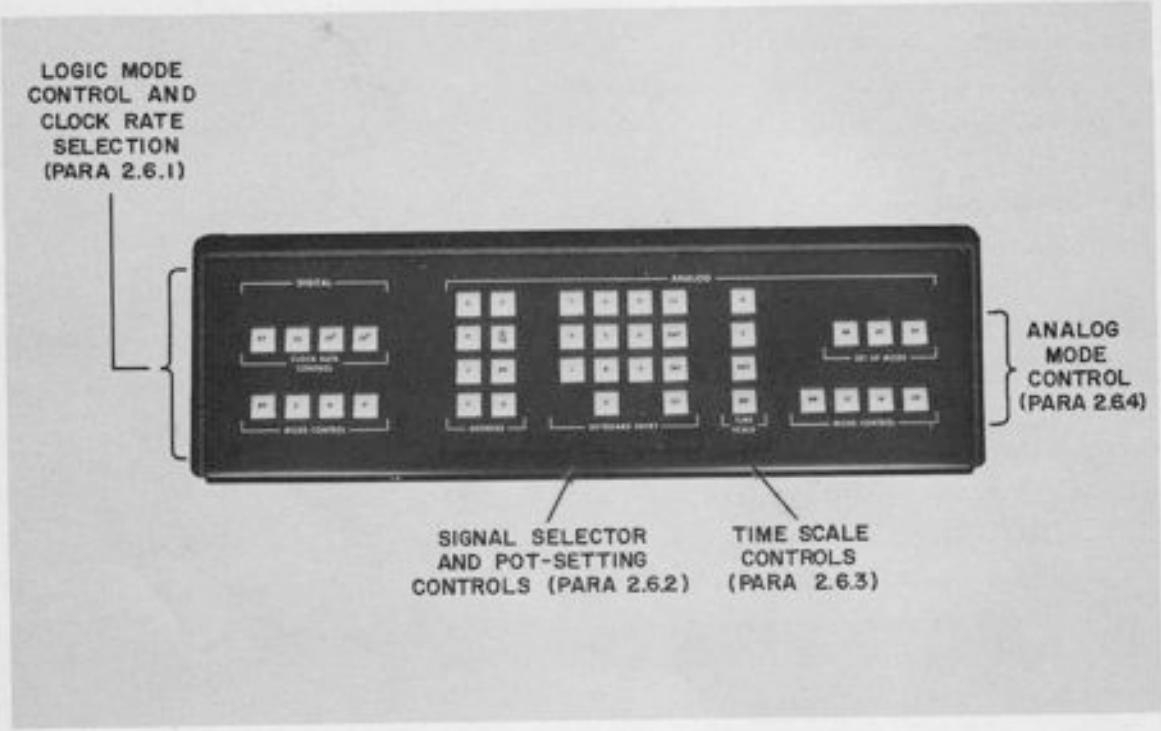


Figure 2.4. The Control Keyboard

The PP button in the logic mode control group allows control of the logic mode by the patch panel. See Chapter 21 for further information.

2.6.2 Signal Selector and Pot-Setting Controls

These controls allow signal selection (i.e., addressing an amplifier or pot for readout by the DVM) and setting of servo-set pots. The entire group consists of 22 buttons: the eight marked

A, P, D, D/10, T, PP, F and Q; the ten numerical keys (marked 0-9); and the four control keys (marked CL, DAC, INC, and GO). The signal selector is described in detail in Chapter 3, and the pot-setting system in Chapter 4.

2.6.3 The Time Scale Controls (N, F, SEC, MS) (See also Chapter 19)

These buttons control the feedback capacitor values on the integrators and the rate at which the rep-op timer runs. The N and F (Normal and Fast) buttons form a mutually exclusive pair; the SEC and MS (Seconds and Milliseconds) form another mutually exclusive pair. Selecting N and SEC provides the standard feedback capacitor value (10 microfarads). This gives a *one-second* time constant when used with the standard "gain one" resistor (100K). Selecting MS instead of SEC decreases the capacitor value by a factor of 1000 (to 0.01 microfarad), providing a 1000-to-1 speedup. Hence, the time constant for a "gain-one" input becomes one *millisecond* when MS is selected.

The "F" (Fast) button provides a 10-to-1 speedup. Thus, when "F" is selected, the time constant becomes 0.1 second or 0.1 millisecond.

Note that the speedup factors of 10 and 1000 are cumulative; in combination they give a speedup of 10,000 to 1.

Each integrator has local controls for the "F" and "MS" selections on the logic panel. Patching into these terminals overrides the master pushbutton control.

2.6.4 Mode Control Buttons (See also Chapter 20)

These seven buttons form a mutually-exclusive set (the computer is in only one of these modes at a time). The modes are as follows:

PC (Pot Coefficient). This is the standard quiescent mode. Every amplifier is provided with feedback by means of a relay, to prevent overloads. Hence, the computer should be in this mode whenever it is "at rest," or unattended. If a pot is addressed in this mode, the pot coefficient (setting) will be displayed (the patched input is switched off and + Reference is applied to the input of any pot which is addressed on the signal selector).

SP (Set Pots). This mode provides feedback for every amplifier to prevent overloads, and also puts reference on the input of an addressed pot. It differs from the *PC* mode in that it is possible to set pots in this mode; that is, the servo setting system is energized (see Chapter

4 for setting procedure). Hence, the *PC* and *SP* modes together correspond to the *pot set* mode on most other computers, except that the use of *two* such modes allows pot coefficient readout (in *PC* mode) without the danger of inadvertently mis-setting a previously set pot. Hence, the *SP* mode should be used *only* during actual pot setting.

ST (Static Test). This mode forces all integrators into the *IC* mode (regardless of local patching). It also energizes the ± Test Reference voltage terminals (see Paragraph 12.5). In addition, it allows derivative readout for integrators and track/store units. (See Paragraphs 6.3.4 and 7.1.3.4.)

IC, H, OP *(Initial Condition, Hold,* and *Operate).* When one of these modes is selected, all integrators are put into that mode *except those that have different mode control logic individually patched.* (See Paragraph 6.3.2.) In addition, certain other functions are normally "slaved" to the mode control (for example, the pen on an X-Y plotter will normally go down only in the *operate* mode, although it is possible to override this feature by local patching).

PP (Patch Panel). When this button is depressed, the mode of the computer is controlled from logic signals on the patch panel. Any of the three computational modes *(IC, H, OP)* may be obtained under logic control. Manual (pushbutton) control may be resumed at any time by selecting any mode manually.

2.7 THE TEST POSITION (See Figure 2.5)

A slot labeled "TEST POSITION" appears at the bottom of the analog readout panel. If an analog tray is inserted in this position, power is applied to it, and it may be tested and adjusted under operating conditions.

2.8 THE VDFG AND LIMITER DRAWERS

To the right of the operator, as he sits at the console, are six slide-out drawers. The uppermost drawer contains the controls for setting the feedback limiters. (The limiters themselves are located in trays behind the patch panel.) Limiters may be easily set without patching modifications; the limit value is read directly on the DVM. Independent controls are provided for the positive and negative limit values on each limiter. The setup procedure is described in Paragraph 12.1.3.

The remaining five drawers contain the variable DFG's. There are a total of 18 ten-segment DFG's, grouped in pairs, so that the two DFG's in any pair may be used as a single twenty-segment unit. The uppermost DFG drawer (the one just below the limiter drawer) contains the DFG setup panel, which allows simplified DFG setup. See Paragraph 10.3 for setup procedure.

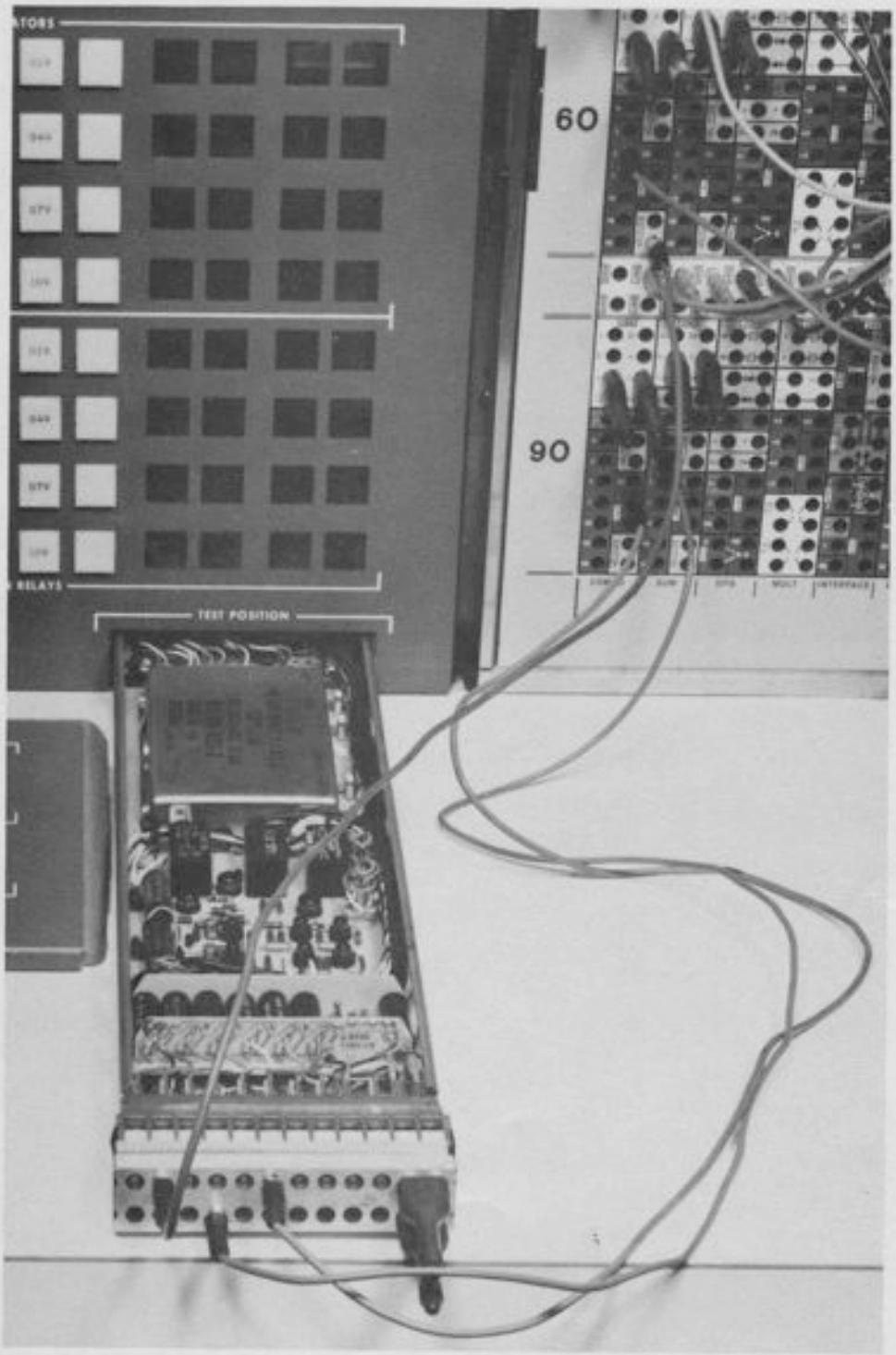


Figure 2.5. A Combination Amplifier in the Test Position

CHAPTER 3

THE SIGNAL SELECTOR SYSTEM

The signal selector is a collection of registers and relays under the control of a keyboard. When a component is addressed, the relays in the signal selector select the output of that component, and its value is displayed on the DVM.

3.1 THE COMPONENT SELECTION KEYS

There are eight keys for selecting the *type* of component addressed. Once a component selection has been made, it remains in force until changed. For example, if A32 has been addressed, and it is desired to read A45, the "A" button need not be depressed a second time.

The eight keys form a mutually-exclusive group; only one type of component may be selected at a given time. The buttons do not light up to indicate which type has been selected; this is unnecessary since the entire address (e.g., A32) is displayed in the DVM windows.

The eight component characters are as follows:

A (Amplifier). This reads the amplifier output. In a fully-expanded machine, all addresses from A0 to A119 represent amplifier outputs (120 addresses).

P (Pot). This address reads the servo-set pots. In the *SP* or *PC* mode, the pot *co-efficient* is displayed (reference voltage is applied to the pot). In all other modes, the pot *output* is displayed (the regular input is connected to the pot). The 120 *servo-set* pots (P0 through P119) are addressed with the letter P; the letter Q is used for handset pots. The servo pot setting system is covered in Chapter 4.

D (Derivative). This address applies to all integrators and track/store units. When a derivative is addressed, the appropriate summing junction is switched from the amplifier to the DVM. The DVM displays the sum of the inputs (multiplied by the appropriate gains) *without sign inversion*. Thus, if +Reference is patched to a gain-of-one on integrator 25, D25 will read +1.0000. An interlock is provided to prevent accidental addressing of a derivative in the *IC* or *OP* modes (see Paragraph 6.3.4 for explanation).

D/10 (Derivative/10). This address performs the same function as the "D" address, but with a change in gain within the DVM. The displayed output is ten times smaller. This address is

used whenever the value of the derivative is too large to be read directly without attenuation. For example, suppose an integrator receives two inputs on gains of one; one input is 0.8000 unit (8 volts) and the other is 0.9000 unit (9 volts).

The sum of the inputs is +1.7000, which would overload the DVM, since the maximum allowable DVM display is 1.1999. By using the "D/10" key, a display of +.1700 is produced, which may be interpreted as a derivative readout of +1.700.

T (Trunk). This key allows readout of any of the 120 trunks (T0 through T119), provided for console-to-console connections, or for tie-in of external equipment. See Paragraph 12.4.

PP (Patch Panel). This key connects the DVM to the DVM input terminal on the patch panel. The letters "PP" are displayed on the DVM, and the numerical address does not matter.

F (Function Generator). This key allows readout of any of the 18 variable DFG's. Only addresses from 32 to 117, and ending in 2 or 7 correspond to DFG's. The output amplifiers for the variable DFG's are built into the DFG's; these amplifiers are the only amplifiers not addressed with the letter "A". The "F" button lights up whenever DFG's are being set up.

Q. This address is used for the handset pots. In the *SP* and *PC* modes, reference is applied to the pot so that the displayed value is the pot *coefficient;* in all other modes, the output is displayed with the actual input connected.

3.2 THE TEN NUMERICAL KEYS (0 through 9)

These keys are used for entering the numerical portion of an address, and also (in the *SP* mode) for entering the desired value for pot-setting. In the *SP* mode, the keyboard alternates between addresses and values. A green light in the DVM display area reminds the operator whether the keyboard is set to interpret the keyboard entry as an address or as a value. When the green light is in the address display area, the keyboard entry is interpreted as an address; when it moves down to the numerical display portion of the DVM, a value is being entered. In all modes except *SP*, the light remains in the Address area, and only addresses may be entered. (An exception to this rule is mentioned in 3.3.2, below.)

Numerical keyboard entries are shifted in from the right; this eliminates the need for entering leading zeros in addresses. For example, A34 and A034 are equivalent addresses, and will address the same amplifier.

3.3 THE CONTROL KEYS (CL, DAC, INC, GO)

These keys are used in conjunction with the numerical entry keys for readout and/or pot setting:

3.3.1 CL (Clear)

This key is used primarily to correct mistakes, and almost exclusively in the *SP* mode. It returns the keyboard to its initial state, ready to accept the first digit of an address. It may be used to terminate the pot setting procedure without actually setting a pot (for example, when an incorrect entry has been made). It is also useful in case a pot fails to set correctly (e.g., due to a servo failure, open winding inside the pot, etc.). In such a case, the servo will continue to attempt to set the pot, and the CLEAR key may be used to disengage the servo and allow further addressing.

3.3.2 DAC (Digital-to-Analog Converter)

This key allows numerical data to be entered into the DAC in modes other than *SP*. (See Paragraph 3.7 for a description of the DAC.) To enter a numerical value, depress the DAC key, enter the value, and depress CLEAR.

3.3.3 INC (Increment)

This key advances the address register to the next sequential address. Thus, if a large number of amplifiers are to be read out in sequence (or a large number of pots set in sequence), it is not necessary to re-enter the complete address each time. This feature is useful for components such as amplifiers, pots, and trunks, whose addresses go from 0 to 119 inclusive. It is not particularly useful for derivatives or function generators, whose addresses are not sequential. For example, DFG addresses end in 2 or 7; the next DFG after F32 is F37, which would require the INC button to be depressed five times. For such components, it is simpler to enter the next address from scratch.

3.3.4 GO

This key serves two functions: acknowledgement of an address and setting a pot. After each address has been entered, the address is displayed in the DVM address display area, but the DVM value is blanked. This means that the address register contains the address of the desired component, but that the readout relay for that component has not actually been energized. Acknowledging the address with the GO key closes the appropriate relay, connecting the addressed component to the DVM. This feature prevents the accidental addressing of components and the consequent display of erroneous values. For example, in addressing A28, the operator

first enters the digit 2, and then the digit 8. After the digit 2 is entered the address register momentarily holds the address A2, but since the GO key has not been depressed, the DVM is blanked, preventing display of the undesired output of amplifier 2.

In the *SP* mode, the GO key also controls the function of the numerical keyboard entry. After a pot address is entered, the GO key is used to acknowledge the address in the usual way, and, in addition, it prepares the keyboard to interpret the next entry as an analog value (desired pot setting). The value is then entered, and the GO key is depressed a second time. This action actually sets the pot, displays its setting on the DVM, and prepares the keyboard to accept a new address. Further details on the pot-setting procedure are given in Chapter 4.

3.4 READOUT PROCEDURES

To read out an amplifier, pot output, DFG, etc., enter the address, and depress GO. The value will be displayed on the DVM. The computer may be in any mode, with the following exceptions:

1. The *SP* mode should be avoided unless it is actually desired to set pots. As mentioned in Paragraph 3.3, the GO key in this mode will prepare the keyboard to interpret the next entry as a pot setting, rather than an address. To read out pot coefficients without disturbing them use the *PC* mode.

2. As pointed out in Paragraph 3.1, the D and D/10 keys do not function in the *IC* and *OP* modes.

3. In the *PC* mode, it is possible to read amplifier outputs, but not very informative, since all amplifiers have a small feedback resistance connected around them in this mode, thus preventing overloads and keeping the output near zero.

3.5 SEQUENTIAL READOUT

Reading out a large number of components is simplified by the fact that the component letter need not be entered as long as it does not change. In addition, the INC key is useful in reading

out components in sequence. For example, to read out A0, A1, A2, A13, A14, A15, A20, F32, F37, and A50, the following sequence would be used:

A0	GO	Address and Output of A0 are Displayed
INC	GO	Address and Output of A1 are Displayed
INC	GO	Address and Output of A2 are Displayed
13	GO	Address and Output of A13 are Displayed
INC	GO	Address and Output of A14 are Displayed
INC	GO	Address and Output of A15 are Displayed
20	GO	Address and Output of A20 are Displayed
F32	GO	Address and Output of F32 are Displayed
37	GO	Address and Output of F37 are Displayed
A50	GO	Address and Output of A50 are Displayed

3.6 PATCH PANEL TERMINALS

Three signal selector outputs are provided on the patch panel, marked ASEL, FSEL, and TSEL. They are located in the strip area below trays 30 and 31. Whenever a component of any kind is addressed, the outputs of the corresponding amplifier, DFG, and trunk terminate at the ASEL, FSEL, and TSEL terminals respectively. For example, addressing A32, P32, or any address whose *numerical* part is 32 will switch the output of A32, F32, and T32 to the appropriate terminals.

Note that not all numerical addresses are valid addresses for variable DFG's. For example, if the numerical part of the address is 34, then A34 and T34 will be connected to the ASEL and TSEL terminals respectively, but nothing will be connected to the FSEL terminal since there is no F34.

Note also that there is no PSEL terminal. This is because pots are not low-impedance outputs. If a PSEL terminal were provided and were patched to a load, there would be danger of inadvertantly loading pots, either during setup, during operation, or both.

The Signal Selector outputs are occasionally useful for selecting different signals for recording on an X-Y plotter, or for general-purpose switching.

3.7 SYSTEM BLOCK DIAGRAM

The operation of the signal selector can be better understood by reference to the simplified block diagram in Figure 3.1. The numerical portion of an address is entered on the ten nu-

merical keys. It is stored in a 3-Digit BCD (Binary-Coded-Decimal) register. The numerical information passes through the circuitry marked "steering logic", which determines whether the information is to be regarded as an address (in which case it is loaded into the address

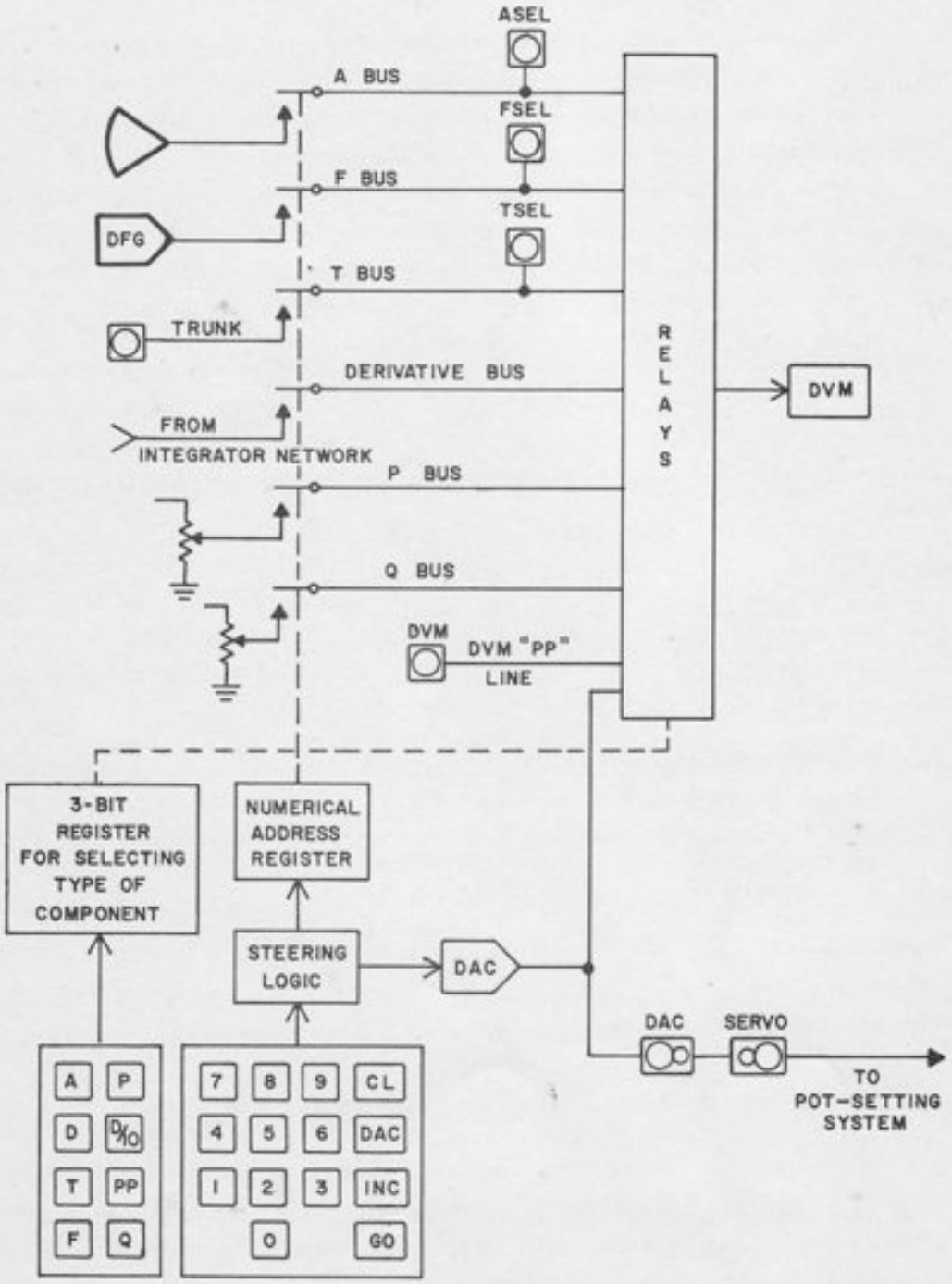


Figure 3.1. Signal Selector, Block Diagram

register) or a numerical value for pot-setting (in which case it is loaded into the DAC). In all modes except *SP*, the information is regarded as an address and loaded into the address register (except that the "DAC" button can override this feature and allow loading of the DAC in any mode).

Once an address has been entered, the address register contains the numerical portion of the address, but the actual readout relays are not energized. Depressing the GO key allows these relays to close. Note that several components with the same *numerical* address (e.g., A32, F32, T32) are addressed simultaneously. The eight selected lines, one for each group of components, pass through a relay matrix, which selects which of the eight lines is actually connected to the DVM. This relay matrix is controlled by another register with eight states (three bits), which stores the information necessary to determine the type of component being addressed.

In the *SP* mode, the GO key not only acknowledges the address, but also triggers the steering logic to allow the next keyboard entry to enter the DAC (Digital-Analog Converter) rather than the address register. The DAC consists of a number of precision resistors connected through relays to an amplifier. The output of this amplifier is a voltage proportional to the numerical entry. The entry 3095 will produce +0.3095 unit (or +3.095 volts) at the DAC output. The voltage is used as one input to a servo amplifier; the other input is the arm of the pot to be set. When the GO key is depressed, the servo is energized, and the pot is set. When the pot output and the DAC output are equal (to within 1 millivolt, or 0.0001 unit), the servo reaches a null and the pot setting is completed. The servo is de-energized, and the steering logic is triggered to allow the next keyboard entry to be interpreted as an address.

Should the servo fail to null, depress the CL button, which will de-energize the servo and terminate the pot setting procedure.

Note that the DAC is amplifier-buffered, and is terminated on the patch panel. This feature allows the use of the DAC as a signal source, or as a low-speed converter for hybrid computation.

During the pot setting procedure, while the numerical value is being loaded into the DAC, the output voltage of the DAC is connected to the DVM, so that it may be monitored, if desired. This feature provides a positive check on the accuracy of the DAC, since its actual analog output is monitored.

A patch panel input marked "SERVO" appears on the patch panel above the "TSEL" terminal beneath tray 31. This terminal permits the setting of a pot against an analog source other than the DAC (for example, a patched trunk input from another computer or an external source). It is connected to the DAC terminal by normally closed patching contacts, so that no patching is needed for normal pot setting operation.

CHAPTER 4

THE SERVO POT-SETTING SYSTEM

The 120 servo-set pots (P0-P119) are set by the servo pot-setting system, part of which has been described in Chapter 3. This chapter gives a more detailed description of the pot-setting system, an explicit set of pot-setting instructions, and a description of the manual adjustment of servo-set pots.

4.1 SETTING A POT FROM THE KEYBOARD

To set a pot from the keyboard, the following steps should be taken:

1. Make sure computer is in *SP* mode.

2. Make sure the POT ADDRESS controls (lower left-hand corner of the analog readout panel) are in the *keyboard* mode. The function of these controls is described in Paragraph 4.4; for the present purposes it is sufficient to know that the *keyboard* mode should be selected for normal operation.

3. Make sure the green light is in the ADDRESS DISPLAY portion of the DVM, (the upper windows). If it is not, depress the CLEAR button. The presence of a green light in the upper window indicates that the keyboard entry will be interpreted as an *address*.

4. Enter the desired address (e.g., P29). Leading zeros may be omitted, but will do no harm if entered (e.g., P029 would address the same pot). Terminate address with GO Key.

5. The green light should now have moved to the lower row of windows (the DVM VALUE display). This indicates that the next keyboard entry will be interpreted as a value. Enter the desired value (4 digits) and depress GO again. This should set the pot and return the green light to the upper row of windows, indicating the keyboard is ready to accept the next address.

6. As the pot sets, a red light may come on momentarily in the lower left-hand window on the DVM. This is a normal indication of the necessary servo error during the setting

process. When the pot is set correctly (to within 0.0001), the light will go out, the servo will be automatically disengaged, the actual pot-setting will be displayed on the DVM, and the keyboard will be ready to accept the address of the next pot to be set.

If the light remains on for any considerable length of time, it is an indication that the pot has not been set correctly (the maximum setting time for maximum pot travel, from 0.0000 to 0.9999, is one second). Depressing the "CL" key will terminate the pot-setting procedure and allow other pots to be set.

4.2 EXAMPLE OF SEQUENTIAL POT-SETTING

Although the explanation in Paragraph 4.1 is somewhat lengthy, the actual process goes quite rapidly. As an example, consider the steps required to set the following pots to the desired values:

P0	3842
P1	9980
P2	0047
P14	5069
P20	4831
P21	1117

The sequence of operations would be as follows:

Select *SP* mode, check to make sure POT ADDRESS control is in *keyboard* mode, and that the green light is in the upper right-hand DVM window (in the ADDRESS DISPLAY area). Then make the following entries:

P0	GO	3842	GO	(This sets P0)
INC	GO	9980	GO	(This sets P1)
INC	GO	0047	GO	(This sets P2)
14	GO	5069	GO	(This sets P14)
20	GO	4831	GO	(This sets P20)
INC	GO	1117	GO	(This sets P21)

Note that some of the pots are in sequence (e.g., P0, P1, P2) and others are not. Note also that even the out-of-sequence pots do not require re-selection of the "P" portion of the address.

If several pots have the same setting, the process can be speeded up by not re-entering the value. For example, the following sequence will set P14, P20, and P21 to .2500:

P14	GO	2500	GO
20	GO		GO
INC	GO		GO

The value .2500, once entered, remains in the DAC until changed. Note, however, that both GO commands are still necessary, even though there is no numerical entry between them.

4.3 MANUAL ADJUSTMENT

Manual adjustment of servo-set pots may be accomplished in any mode by means of the POT CONTROL lever, located below the DVM on the analog readout panel. To use this control, proceed as follows:

1. Address the pot, either with the regular signal selector or with the MANUAL POT ADDRESS system. (See Paragraph 4.4.)

2. Move the POT CONTROL lever to the left (to decrease the setting) or to the right (to increase it). The pot will move at a rate dependent upon the amount of deflection; the rate can be varied from a very small value (slow enough to adjust the last decimal place) up to a maximum of about 4% per second (i.e., full-scale travel takes about 25 seconds).

It is suggested that the operator address a pot (any pot) in the *PC* mode, and adjust it manually at several different rates, to familiarize himself with the process and get the "feel" of the system. This feature is very handy for adjusting parameters in rep-op, while observing the effect on a scope.

Note that, since the manual adjustment can take place in any mode, including *operate* and *repetitive operation*, it may be adjusted manually while the problem is running, and without removing the patched input to the pot.

If the pot reaches the extreme end of its travel (0.0000 or 0.9999) during manual adjustment, it will simply stop there. It is impossible to cause electrical or mechanical damage by overdriving it. The POT CONTROL lever is spring-loaded, so that, when released, it returns to its center position. (OFF).

4.4 MANUAL ADDRESSING

In addition to the manual setting feature, provision is also included for manual *addressing* of a servo-set pot while observing the output of some *other* component (e.g., an amplifier or DFG) on the DVM. This requires some method of by-passing the signal selector.

The manual pot addressing system consists of a pair of thumbwheels marked "MANUAL SELECTOR" in the lower left-hand corner of the analog readout panel. These thumbwheels are under the control of the two pushbuttons directly above, marked "POT ADDRESS." These pushbuttons form a mutually-exclusive pair: the pot address is either MANUAL or KEYBOARD, but not both. In the *keyboard* mode, the pot address comes from the keyboard, allowing normal pot-setting. In the *manual* mode, the pot address comes from the manually-set thumbwheels. The first thumbwheel has twelve positions (0-11), and the second has ten (0-9). Hence, any pot from P0 to P119 can be manually addressed, freeing the signal selector for addressing some other component in the conventional manner. Note that the manual selector selects the pot *for setting purposes only*, not for display.

After manual pot-setting is completed, the operator should return the POT ADDRESS to *keyboard* to allow conventional servo-setting once more. If this is not done, and a pot is addressed on the keyboard while the POT ADDRESS control is in the *manual* mode, a red light will appear in the "P" window in the DVM address display, warning the operator that the pot he has just entered is not really being addressed.

4.5 CIRCUIT DETAILS

4.5.1 Overall Logic Diagram

The diagram given in Figure 4.1 is not intended to be an accurate reproduction of the actual circuitry, but it gives a visual summary of the main paths of information flow and the logic functions performed by the various controls.

There are two sources of pot addresses: the numerical address register which is loaded from the keyboard and the manual selector (the thumbwheels). The "POT ADDRESS" group of pushbuttons determines which of the two addresses - the MANUAL or the KEYBOARD address - will actually be used to set the pot.

A logic signal called "SET POT" in Figure 4.1, is generated by the GO key and additional logic associated with the ADDRESS/VALUE FLIP-FLOP. When this flip-flop is set, the numerical

keyboard entries are interpreted as values, and entered into the DAC (see Figure 3.1). When this flip-flop is reset, numerical entries are interpreted as addresses and loaded into the address register.

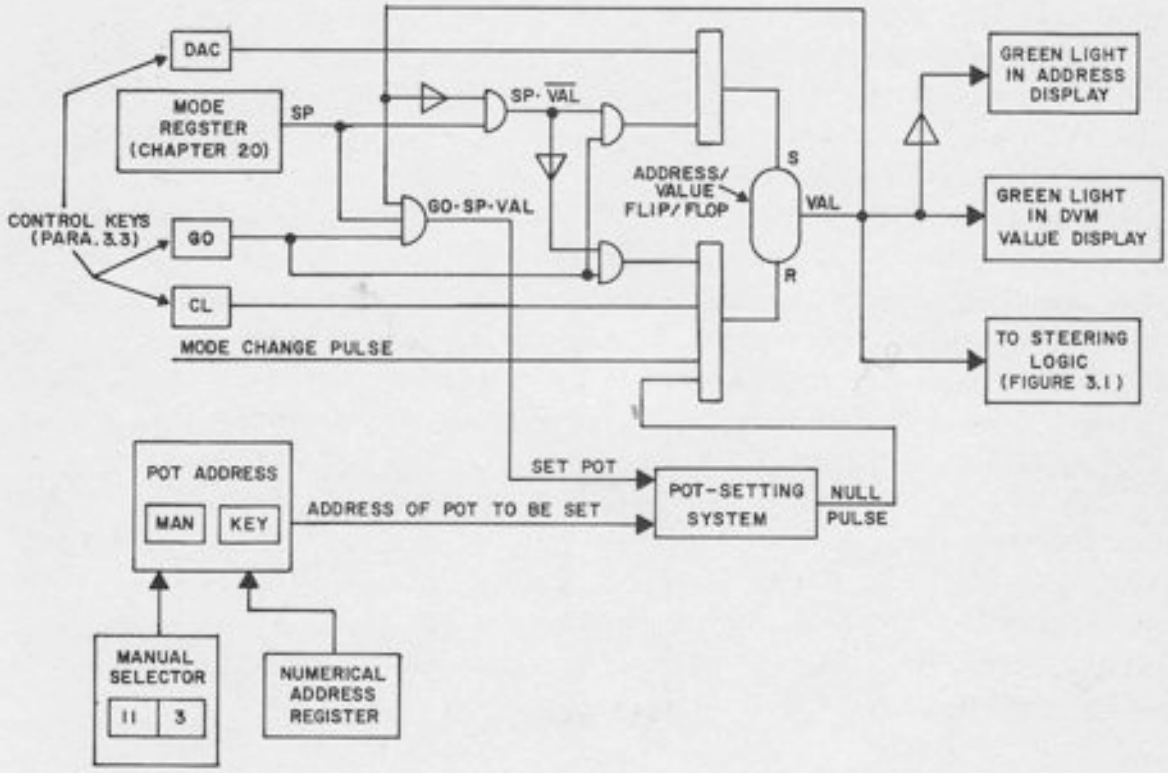


Figure 4.1. Logic Diagram of Servo Pot-Setting System

Note that a mode change pulse (generated on leaving the *SP* mode) will clear the flip-flop. In all modes except *SP*, the flip-flop remains reset, so that entries are normally interpreted as a addresses. However, in the *SP* mode, the GO signal causes the flip-flop to alternate between the address and value states. When it is in the value state, and the value has been entered, depressing the GO key generates a "SET POT" logic signal, which causes the pot to be set. After the setting is completed, the servo system sends out a null pulse (indicating a null at the output of the servo amplifier), which resets the flip-flop, preparing the system for the next pot address.

The DAC and CLEAR buttons allow certain modifications of this basic sequence. The "DAC" button allows the flip-flop to be set, and hence the DAC to be loaded, in any mode. The "CLEAR" button allows resetting (clearing) of the flip-flop in any mode, at any point in the sequence.

4.5.2 Individual Pot Addressing Circuitry

The pot addressing circuitry is given in Figure 4.2. Each pot has a relay which is energized whenever the pot is addressed. The relay is shown de-energized in Figure 4.2 (i.e., with the pot *not* addressed). Note that the pot is connected to its patch panel input terminal through contacts on the pot address relay. When this relay is energized, the pot input is connected to an external relay which either re-connects it to the patch panel input terminal or connects it to + Reference, depending on the computer mode.

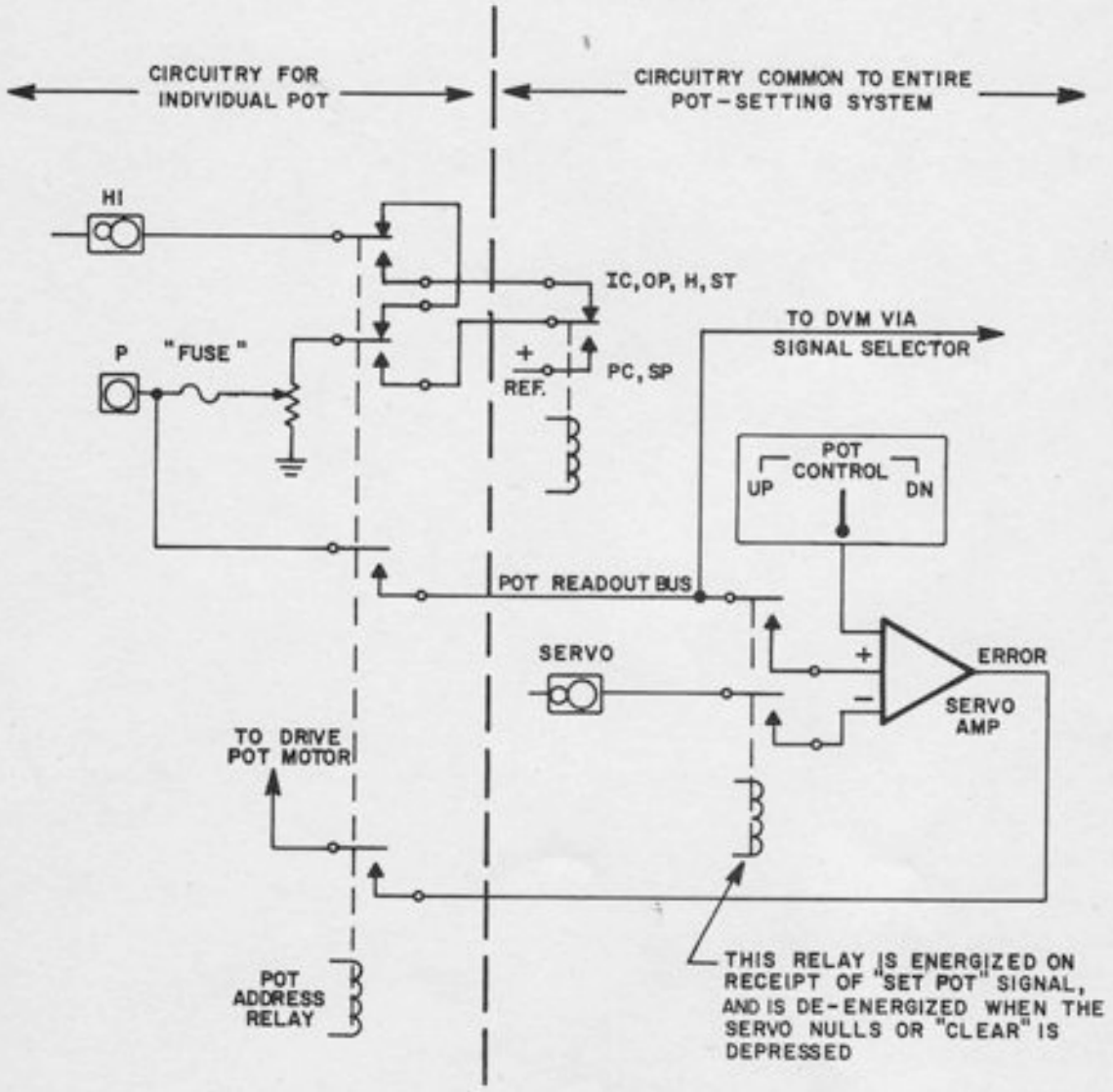


Figure 4.2. Individual Pot Addressing Circuitry

Another set of contacts on the relay puts the output of the pot on the readout line for connection to the DVM, and another set of contacts connects the output of the servo amplifier to the pot motor, allowing the pot to be set.

When a "SET POT" logical signal is received from the keyboard (see Figure 4.1) the pot output and the SERVO input are connected to the servo amplifier, generating an error signal which drives the pot until the amplifier nulls - i.e., until the pot output equals the SERVO input. The SERVO input, as described in Chapter 3, is terminated on the patch panel, and normally connected to the DAC output. Hence, if nothing is patched in, the pot is set to the value on the DAC, which has been previously entered on the keyboard.

In modes other than *SP*, the pot may be set by addressing it (either manually or by keyboard) and moving the POT CONTROL lever manually. This lever puts a small signal into the servo amplifier, which drives the pot up or down at a rate dependent on the deflection of the lever.

CHAPTER 5

PATCH PANEL LAYOUT

For ease in programming, assigning components, and locating components for patching, the 680 patch panel is arranged in a symmetric manner. The analog portion of the patch panel is divided into 24 nearly-identical areas called *fields*. Thus, the programmer need only learn the basic pattern for a single field.

5.1 THE TRAY

Each field on the 680 patch panel is divided into five *trays*. The tray is the basic 680 patching area, and contains a number of closely related components. As its name implies, a tray area corresponds to an actual tray in which most of the components are located. A typical tray and its corresponding patching area (2 holes wide, 12 holes high) are shown in Figure 5.1.

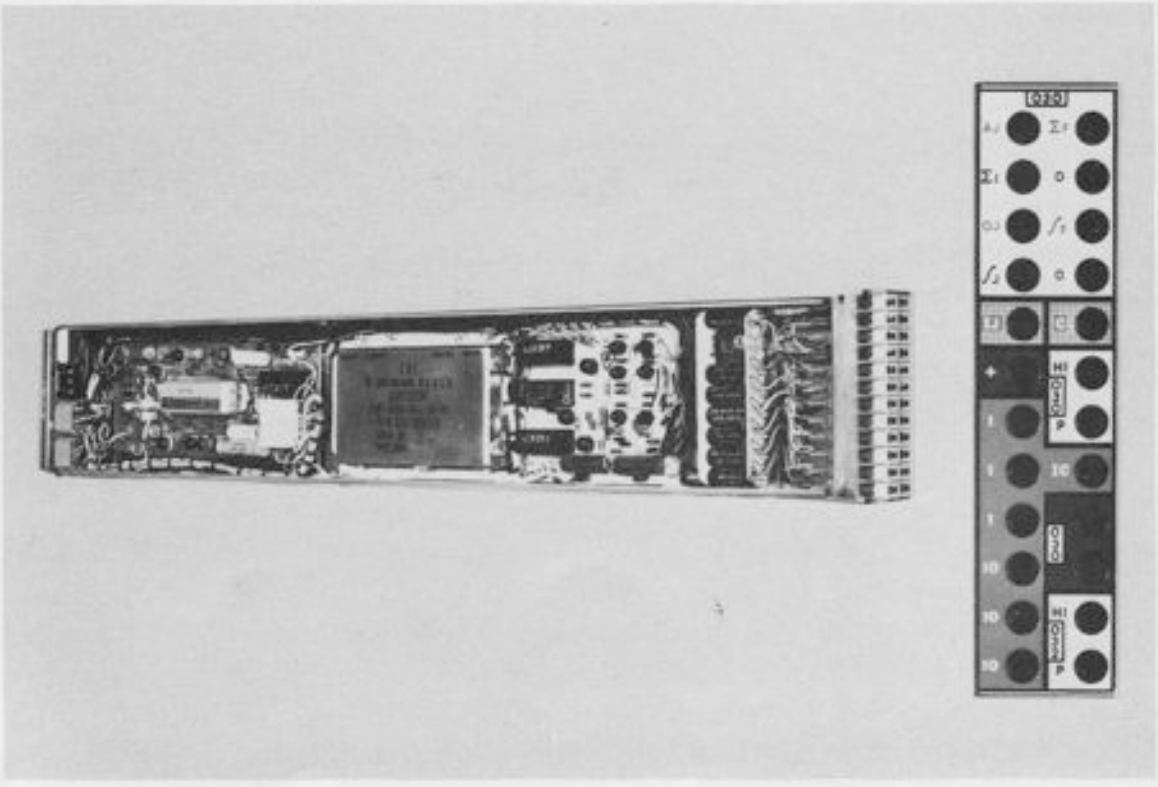


Figure 5.1. A Typical Tray and its Patching Area

The trays are easily removable from the front of the computer. They have connectors on the back for the necessary power supply voltages and other inputs. The connections on the front make up the patch bay, into which the patch panel is inserted.

In the interest of compactness, simplicity of construction, and dynamic response, almost all computing components are located in these trays directly behind the patch panel. The only remotely located components are the potentiometers, the variable DFG's and their associated amplifiers, and the largest feedback capacitors for the integrators.

Components located in the trays directly behind the patch panel include all amplifiers except those associated with variable DFG's; all computing resistors and mode control networks associated with these amplifiers; all fixed DFG's (log/exponential or sine/cosine generators); all multipliers, comparators, electronic switches, and limiters. Locating the components directly behind the patch panel allows termination of their summing junctions on the patch panel for flexibility in patching, without the usual deterioration in performance resulting from trunking the summing junction of a remotely located amplifier up to the panel through many feet of cable. The only amplifiers whose summing junctions do *not* appear on the patch panel are the amplifiers associated with the variable DFG's. The variable DFG's are located in slideout drawers to the right of the operator as he sits at the console; their associated amplifiers are located in the same drawers, again eliminating the need for long summing junction leads. When a variable DFG is not in use, its output amplifier is available for use as an inverter.

5.2 ROWS, STRIPS, AND FIELDS

The patch panel is divided into five horizontal *rows* of 30 trays each. Between rows of trays, there are horizontal *strips* or *bars*, two holes high. In the strip area are located the trunks, reference terminations, ground, plotter and scope connections, the noise generator outputs, DVM patch panel input, and similar miscellaneous terminations (Figure 5.2).

The upper row and the strip immediately below it are devoted to logic elements (flip-flops, registers, gates, etc.). The remaining four rows and three strips are devoted to analog signals. A plastic insert in each logic terminal prevents the use of analog patchcords in the logic area or logic patchcords in the analog area, virtually eliminating the possibility of accidentally patching an analog signal to a logic component. In addition, the use of a ten-volt reference means that even the accidental shorting together or an analog cord and a logic cord will not normally cause any permanent damage. (The logic ONE level is nominally +5 volts.)

A glance at Figure 5.2 will show that there are four times as many analog trays as logic trays. The logic row contains 6 fields of 5 trays each for a total of 30 trays; the analog area has four

such rows, giving a total of 24 analog fields of 5 trays each (120 analog trays in all). The analog trays are numbered sequentially from 0 to 119.

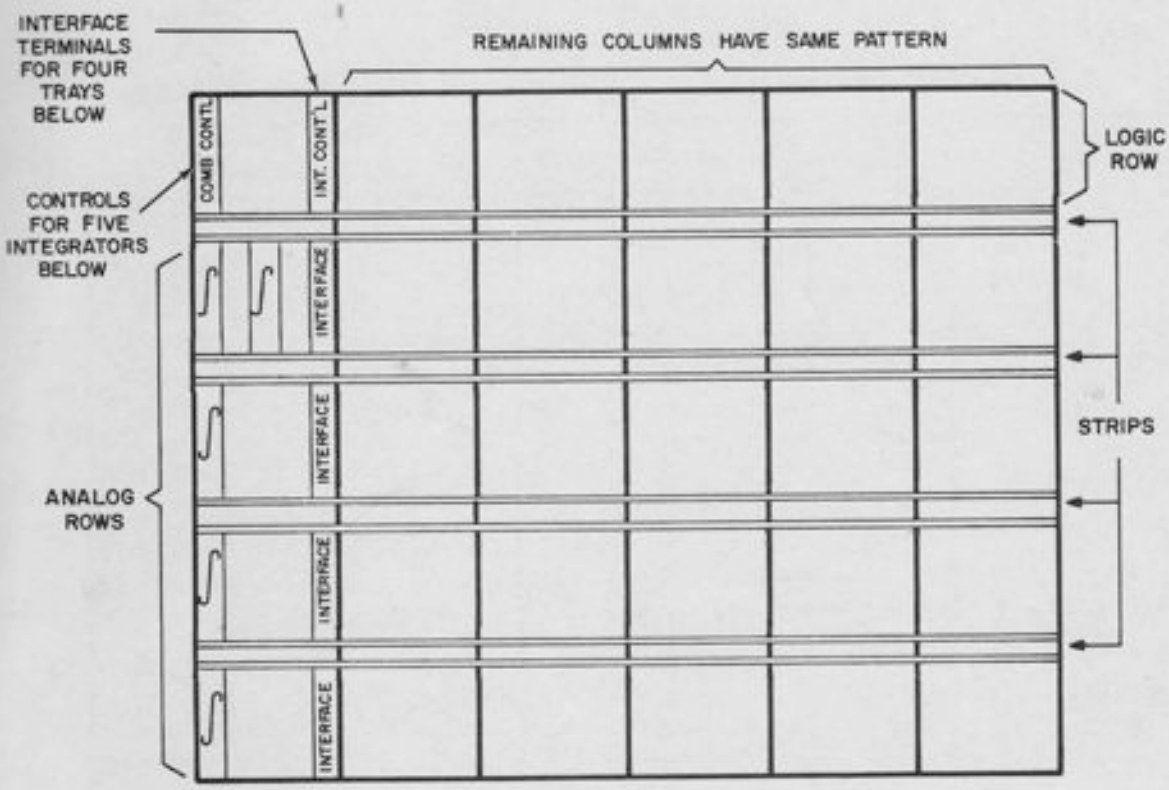


Figure 5.2. Patch Panel Layout, Showing Rows, Strips, and Fields

5.3 THE TYPICAL ANALOG FIELD (Figure 5.3)

As mentioned in Paragraph 5.1, the analog field contains five trays. Each tray is named after the principal type of component (or components) it contains. The five types of trays are as follows:

Tray 0 or 5 is a COMBO tray. Its principal component is a combination amplifier (which can be used as an integrator or a summer).

Tray 1 or 6 is a SUMMER tray. Its principal component is a summing amplifier.

Tray 2 or 7 is a DFG tray, except as noted below. It contains the terminations for a ten-segment variable DFG (which is remotely located), and one or two fixed DFG's (located in the tray). Either a single sine/cosine generator or *two* independent log/exponential DFG's can be put into a single DFG tray. In addition, each DFG tray contains an amplifier, which may be used either as an inverter or as the output amplifier for one of the fixed DFG's (the variable DFG's have their own built-in output amplifiers).

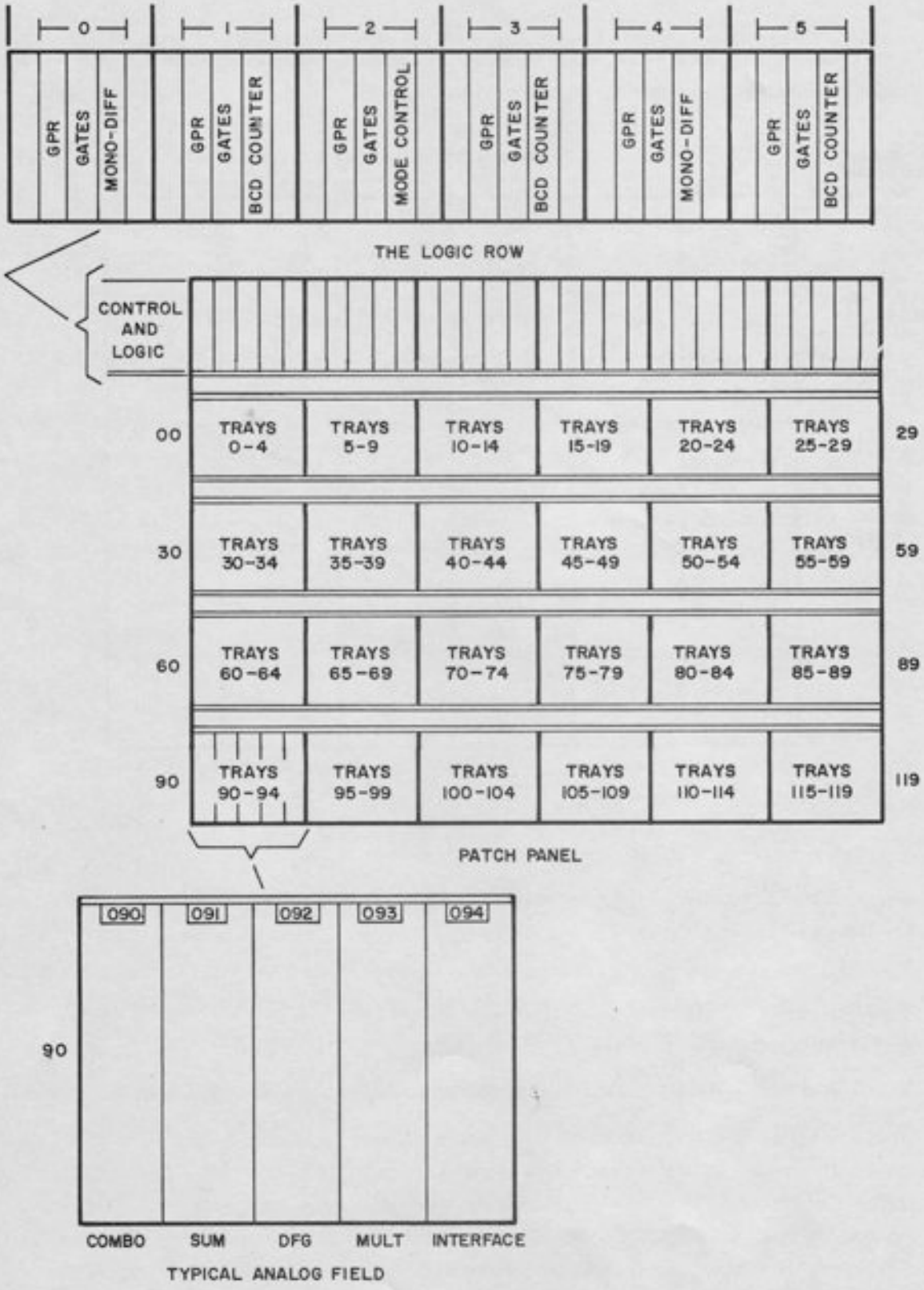


Figure 5.3. Detailed Patch Panel Layout

Tray 3 or 8 is a MULTIPLIER tray. It contains a quarter-square multiplier together with its output amplifier. The output amplifier may be disconnected from the multiplier if desired.

Tray 4 or 9 is an INTERFACE tray. It contains the components that interface with the logic area (an electronic comparator, an electronic switch, and a relay which may be positioned by logic signals). The logic terminations for this tray are in the logic tray immediately above. In addition, an interface tray contains an amplifier, which is not an interface element.

Note that the basic pattern (COMBO, SUM, DFG, MULT, INTERFACE) is spelled out on the patch panel immediately below each field. This pattern is the key to understanding the patch panel organization. The pattern is repeated, with only minor variations, from one field to the next. Since a field contains five trays, the addresses of similar components will be congruent modulo five, that is, integrators end in 0 to 5 (e.g., A0, A5, A25, A30 are all integrators). Summers end in 1 or 6 (e.g., A11, A26, A91, etc.). The only major exception to this rule is in the "DFG" trays in the upper analog row; that is, trays 2, 7, 12, 17, 22, and 27. In order to provide for a balanced complement of equipment, these trays contain additional combination amplifiers (summer/integrators) instead of DFG's.

To summarize, the pattern of analog trays is as follows:

Trays ending in -0 or -5 are COMBO trays.
Trays ending in -1 or -6 are SUMMER trays.
Trays ending in -2 or -7 are either COMBO trays (2-27) or DFG trays (32-117).
Trays ending in -3 or -8 are MULTIPLIER trays.
Trays ending in -4 or -9 are INTERFACE trays.

5.4 THE LOGIC ROW

The logic components, like the analog components, are arranged in as symmetric a manner as possible. There are 6 fields of 5 trays each, for a total of 30 trays (Figure 5.3). Four out of five trays are identical from one field to the next. The general pattern is as follows:

The first tray in each field tray is an INTEGRATOR CONTROL tray; it contains the individual mode controls and time scale controls for the integrators beneath it on the patch panel.

The next tray is a REGISTER tray; it contains a four-bit register which may be used as a shift register, a counter, or as four independent flip-flops.

The next tray is a GATE tray; it contains five general-purpose AND gates.

The next tray is the one that varies from one field to the next.

The last tray is an INTERFACE tray; it contains the logic terminals for the comparators, electronic switches, and relays in the four analog trays directly below it.

Note the similarity between the patterns of the typical analog field and the typical logic field. Both contain five trays, beginning with an integrator tray and ending with an interface tray. The logic trays for integrator control and for interface correspond with the analog trays directly beneath.

There are two exceptions to this direct vertical correspondence, both in the integrator control tray. The first exception refers to the six "extra" integrators in the upper analog row; they share their mode and time scale control with the integrators on their left (e.g., A2 is controlled by the same mode control logic as A0; A7 is controlled by the same logic as A5, etc. The second exception refers to the controls for the track/store units (12 of the 24 summers have built-in track/store networks). These track/store networks are located in the integrator control tray, even though the track/store summer is not *directly* beneath this tray. Track/store units in the first two analog rows are controlled by terminals in the integrator tray above the summer and slightly to the *left;* the controls for track/store units in the lower two analog rows are above the amplifier and slightly to the *right*.

In addition to the above-mentioned controls, the integrator control tray contains a general-purpose two-input AND gate, which is not directly connected to any components in the analog area.

5.5 SUMMARY OF EQUIPMENT COMPLEMENT

The equipment complement of a fully-expanded 680 is as follows:

Amplifiers	156
Servo-Set Pots	120
Hand-Set Pots	12
Multipliers	24
Variable DFG's	18
Fixed DFG Trays*	18
Comparators, D/A Switches, Relay	24

**Each DFG tray may contain <u>one</u> sin/cos generator or <u>two</u> log/exponential generators.*

The complement of amplifiers may be further broken down as follows:

Combination Integrator/Summers	30
Summers	24
Output Amplifiers for Multipliers	24
Junction Inverters	42
Total Amplifiers in Trays	120
Variable DFG Amplifiers (2 per DFG, located in Drawers with the DFG's	36
Total Amplifiers	156

CHAPTER 6

THE COMBINATION AMPLIFIER

6.1 LOCATION AND ADDRESSING

A fully-expanded 680 has 30 combination amplifiers, which may be used as integrators or as summers. (Certain other applications, such as track/store unit, high-gain amplifier, etc., are discussed in Appendix 1.)

All amplifiers whose address ends in -0 or -5 are combination amplifiers. This is a total of 24 combination amplifiers, from A0 to A115. Each of these amplifiers has a set of terminals on the logic panel to allow for selection of the mode (*IC, hold,* or *operate*) from logic signals independent of the main computer mode control. Another pair of terminals allows selection of any of the four feedback capacitor values for the integrator by means of logic signals.

In addition to the 24 listed above, the 6 amplifiers in the upper analog row whose address ends in -2 or -7 are also combination amplifiers (A2, A7, A12, A17, A22, and A27). These amplifiers do not have independent mode and time scale control; each of these amplifiers is controlled by the same logic signals as the combination amplifier to its left. Thus the controls for A0 control A2 also; the controls for A5 control A7 also, etc.

In assigning components for a problem in which some integrators have mode control different from that of the main computer, the integrators in the upper row should be used for large blocks of amplifiers with common mode control. This assignment reduces the amount of patching required, since each patched logic signal controls two integrators. If a particular integrator requires logic control different from that of any other integrator, that integrator should be chosen from the lower three rows.

6.2 PATCH PANEL LAYOUT

The patch panel layout for a combination amplifier is shown in Figure 6.1. Note that a single logic tray contains controls for five combination amplifiers. The upper set of terminals controls two combination amplifiers in the first analog row, the remaining sets of terminals control one combination amplifier each.

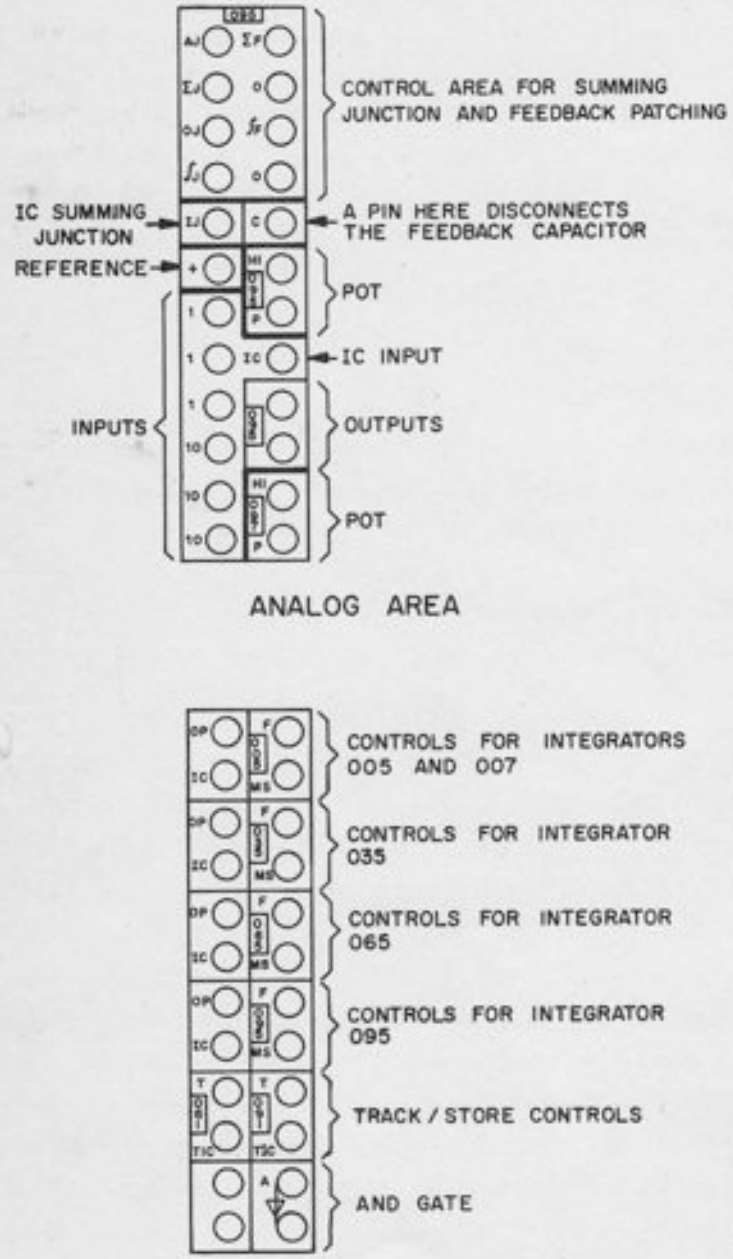


Figure 6.1. Patch Panel Layout for Combination Amplifier

Patching diagrams are given in Appendix 1. A detailed explanation of the terminals and schematic diagrams are given in Paragraph 6.5. For the simplest and most common applications, it is sufficient to know that the upper white area (eight holes) contains the necessary summing

junction and feedback connections to determine whether the amplifier is to be a summer or an integrator. In line with the philosophy of minimizing setup patching, (see Chapter 5) the patch panel is laid out so that one patching action (with a double vertical plug) is all that is required to determine the mode of operation. If this plug is at the top of the white control area, the amplifier is a summer; moving it to the bottom makes the amplifier an integrator. As a mnemonic aid, note that a synonym for top is "summit". Hence, a double-vertical plug at the *top* of the tray makes the amplifier a *summer*. The same pattern is used with the track/store summer and the limit summer; see Chapter 7 for details.

6.3 APPLICATIONS

In addition to being used as a summer or an integrator, the combination amplifier may be used as an electronic switch, a track/store unit, and in several other ways. Appropriate patching diagrams and symbols are given in Appendix 1.

6.4 MODE CONTROL AND CAPACITOR SELECTION

6.4.1 Mode Control

The two terminals marked "IC" and "OP" allow logic selection of any of the three computational modes: *IC*, *hold*, and *operate*. When either of the inputs is high (logic ONE) and the other is low, the integrator will be in the appropriate mode (i.e., a ONE in the IC terminal and a ZERO in the OP terminal will produce the *IC* mode, and vice versa). If both inputs are low (logic ZERO), then the integrator is in the *hold* mode. (This may be remembered by noting that if the integrator is not in *IC* and not in *OP*, then it must be in *hold*.) Finally, if both inputs are high, the *IC* mode results (the *IC* mode command overrides the *OP* command). This information may be summarized in the following table:

IC Input	OP Input	Resulting Mode
1	Any	IC
0	1	OP
0	0	Hold

If nothing is patched into the IC and OP terminals, then they are automatically connected to the master mode control buses; thus the integrator normally has the same mode as the computer unless logic signals are patched in to override the computer mode.

Additional information on the mode control switching is given in Paragraph 6.5. A detailed description of the master mode control is given in Chapter 20.

6.4.2 Capacitor Selection

Capacitor selection, also called time scale control, is determined by the terminals marked "F" and "MS". A logic ONE into either of these terminals speeds up the rate of integration by changing the feedback capacitor. The "F" terminal provides a 10-1 speedup; the "MS" terminal provides a 1000-1 speedup, and together they provide a 10,000-1 speedup.

The availability of four different feedback capacitor values for every integrator is useful for solving problems with a wide range of time constants, for high-speed repetitive and iterative operation, and for many other applications. The fact that these capacitors may be individually selected by logic levels allows automatic re-scaling during problem solution.

The normal feedback capacitor is 10 microfarads; together with the standard "gain-one" (100K) resistor, it produces a one-second time constant. The terminals "F" (FAST) and "MS" (MILLISECONDS) should be interpreted relative to this standard time-constant; the "MS" input makes the time-constant one *millisecond* instead of one *second*, and the "F" input makes it ten-times faster (0.1 second or 0.1 millisecond). This information is summed up in the following table:

"F" Input	"MS" Input	Integrator Rate	Time Constant (With 100K)	Capacitor Value
0	0	Normal Seconds	1.0 SEC	10μF
0	1	Normal Milliseconds	1.0 MS	0.01μF
1	0	Fast Seconds	0.1 SEC	1.0μF
1	1	Fast Milliseconds	0.1 MS	0.001μF

If nothing is patched into these terminals, they are normally connected to master time scale buses, permitting speedup of the entire computer by logical command or by pushbutton. See Chapter 21 for details.

6.5 CIRCUIT DETAILS

A simplified schematic of a combination amplifier is given in Figure 6.2. Its major parts are a high-gain amplifier, a set of feedback capacitors, electronic gates and relays for mode control and readout, an input resistor network, and an IC resistor network.

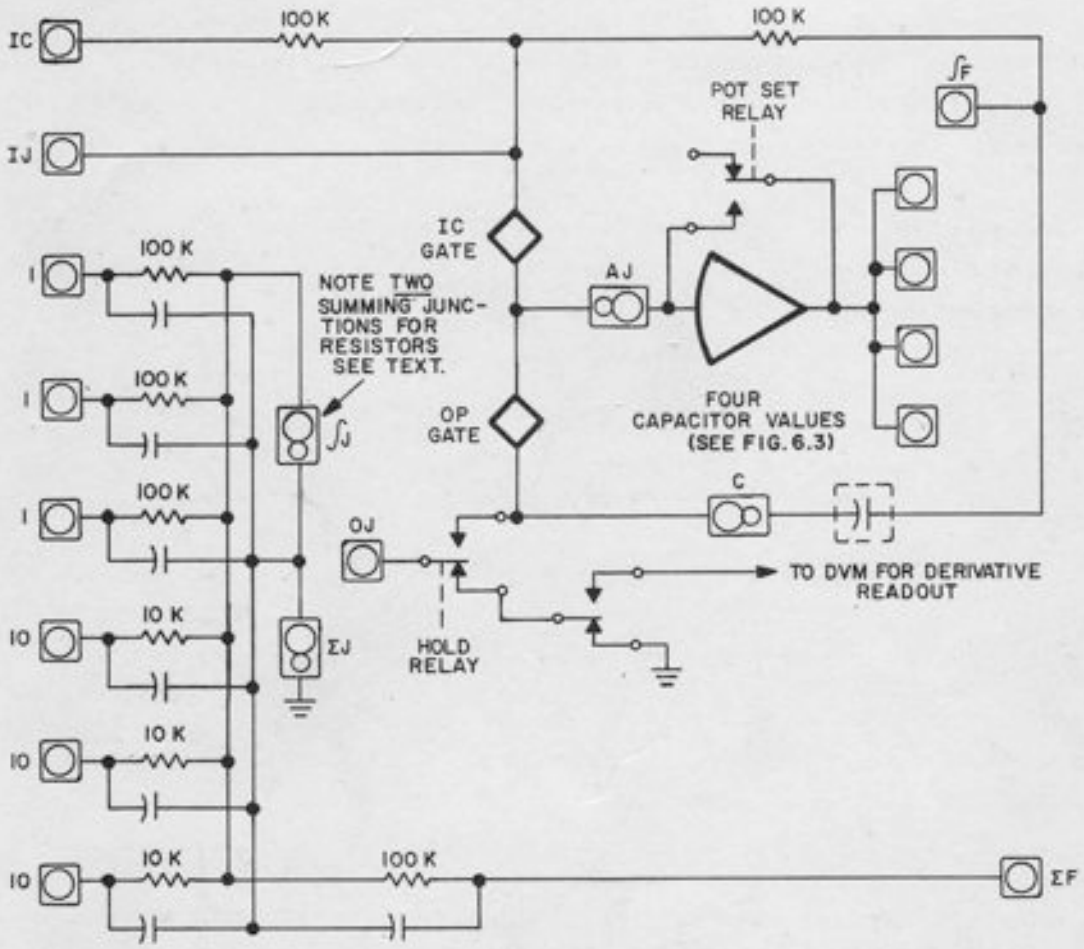


Figure 6.2. Simplified Schematic of a Combination Amplifier

6.5.1 The Junction and Feedback Terminals

The IJ (IC summing junction) and the OJ (OPERATE summing junction) both terminate on the patch panel. These junctions are electronically connected to the amplifier junction in the corresponding mode. In the *operate* mode, the OJ is connected to the amplifier junction and the IJ is grounded (by the IC gate), which assures proper loading on the IC input(s). In the *IC* mode, the IJ is connected to the amplifier and the OJ is grounded by the OPERATE gate, thus allowing the feedback capacitor to charge to the appropriate IC value.

The AJ (Amplifier Junction) is connected directly to the amplifier. Patching into this terminal disconnects the IC and OP gates and allows the use of the amplifier as a summer.

The input resistor network contains seven resistors, including the feedback resistor (note that the feedback resistor is connected to the same junction as the input resistors; it may be used as

an additional "gain one" input resistor when the amplifier is used as an integrator). Two summing junctions are provided for the input resistors: one with capacitors and one without. The ∫J should be used for an integrator, and the ΣJ for a summer.

The reason for two junctions is that the dynamic behavior of a summer is improved by the addition of small capacitors in parallel with the input and feedback resistors, but these capacitors should be removed for an integrator. The reader should be able to verify from Figure 6.2 that inserting a patchcord or a plug into the ∫J terminal leaves the capacitors grounded (so that they are effectively out of the circuit), and inserting it into the ΣJ terminal leaves them in parallel with the input resistors. If it is desired to "borrow" this network for use with another amplifier, this distinction should be kept in mind, and the appropriate junction used. When the network is used with its own associated amplifier, the connection is taken care of by the bottle plug.

The ΣF (Summing Feedback) and ∫F (Integrator Feedback) terminals are for connection to the amplifier output. The integrator feedback consists of a capacitor (whose value may be selected by patched logic signals) and an IC network. The summer feedback is, of course, a resistor. Note that the IC feedback and input resistors are 100K. This is the standard "gain 1" resistor for IC's as well as for regular inputs.

Provision is made for removing all capacitors by inserting a pin in the "C" terminal. Disconnecting the capacitor allows use of the mode control gates for general-purpose electronic switching.

6.5.2 Capacitor Selection

Figure 6.3 is a simplified schematic of the capacitor selection logic. A table giving the capacitor value as a function of the logic inputs is given in Paragraph 6.4. Note that the capacitor values are *additive;* every capacitor value (except the smallest) is achieved by a parallel combination of two or more capacitors. All capacitors not in use are connected through resistors to ground, so that they track the amplifier output at all times, even when not in the feedback loop; this feature is important for automatic re-scaling without loss of signal.

6.5.3 Derivative Readout

Each 680 integrator has provision for derivative readout. The derivative of an integrator is simply the sum of its rate inputs. For example, if an integrator has as inputs +0.0500 unit on a gain of 10, +0.7000 unit on a gain of 1, and -0.3000 unit on a gain of 1, the derivative readout would be $(0.0500 \times 10) + (0.7000 \times 1) - (0.3000 \times 1) = +0.9000$ unit. Note there is no

sign inversion. The derivative readout is achieved by means of the derivative readout relay contacts (see Figure 6.2) which connect the OJ to the derivative readout bus when the amplifier is selected. The derivative readout bus is connected directly to the summing junction of the DVM when the "D" Key is depressed. Since derivative readout breaks the computing loop (the integrator is not receiving its appropriate inputs), it should not be attempted in the *operate* mode. In addition, switching transients may cause errors if the computer is switched from *IC* to *operate* while a derivative is being addressed. Hence, the circuitry is arranged to prevent derivative readout in these modes. Derivatives may be read out only in the *static test* and *hold* modes.

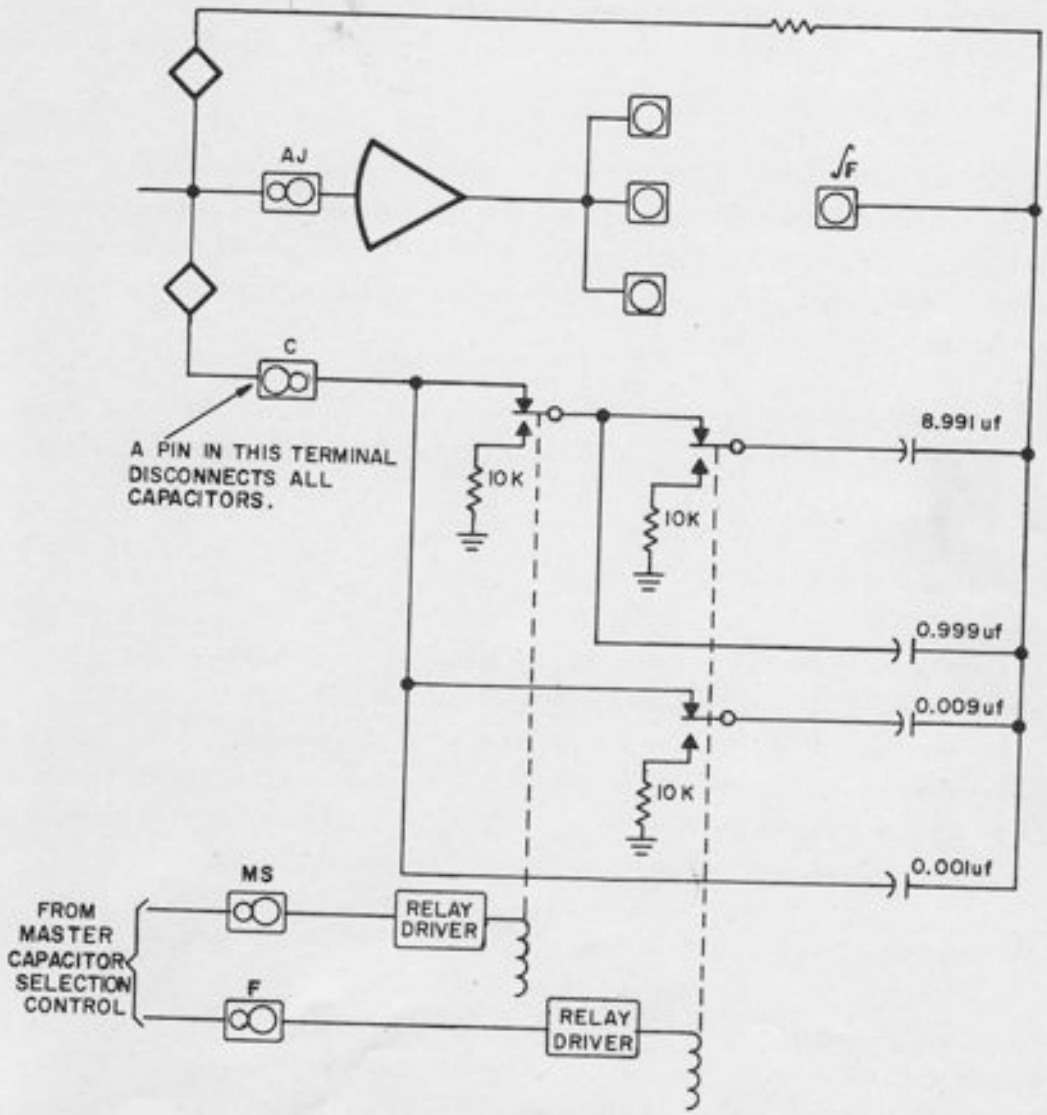


Figure 6.3. Simplified Schematic of Capacitor Selection Circuitry

CHAPTER 7

THE SUMMER

A fully-expanded 680 has 24 summers, one per field. The address of a summer ends in -1 or -6. Each summer has six inputs (three gain-one inputs and three gain-ten inputs). The summers are of two types: the track/store summer and the limit summer. In addition to regular summation, the track/store summer has the ability to track and store one or more input variables under logical control; the limit summer has a built-in limiting network that may be used to generate accurate absolute values and other nonlinear functions.

When used as ordinary summers, the two types are patched identically; a double-vertical plug in the top of the patching area makes either amplifier perform as a summer. Note that the same is true of the combination amplifier as well (see Paragraph 6.2). All summers whose addresses end in -1 are track/store summers; those whose addresses end in -6 are limit summers.

7.1 THE TRACK/STORE SUMMER

7.1.1 Location and Addressing

All amplifiers whose addresses end in -1 are track/store summers; a total of 12 track/store summers in a fully-expanded computer. Each track/store summer has two logic controls in the logic patching area, marked "T" and "TIC". These controls are located in the integrator control tray above the track/store summer and slightly to the left (for a track/store summer in the upper two analog rows) or slightly to the right (for a track/store summer in the lower two analog rows).

7.1.2 Applications

If the amplifier is to be used as an ordinary summer, ignoring the track/store feature, a double vertical plug is inserted in the four terminals at the top of the patching area (Figure 7.1). The logic terminals may be left alone; they have no effect when the amplifier is used as a summer.

Moving the bottle plug one row down (to the bottom of the six-hole control area) converts the amplifier to a track/store unit. The track/store unit has three modes, *track*, *store*, and *IC*, all under logical control. In the *track* mode, the unit acts as an ordinary summer (the output

is minus the sum of the inputs). The unit uses the same input and feedback resistors as does a summer; thus a "1" input produces a gain-of-one, and a "10" input produces a gain-of-ten. With a slightly different patching, other feedback can be used, including pot feedback and even non-linear feedback; see Appendix 1 for details.

In the *store* mode, the output of the amplifier remains constant; thus it stores the value it had when it changed from *track* to *store*. In the *IC* mode, the output is minus the voltage patched into the IC input (just as with an integrator). This mode is useful in the checkout, and in starting off an iterative problem with arbitrary initial parameter values.

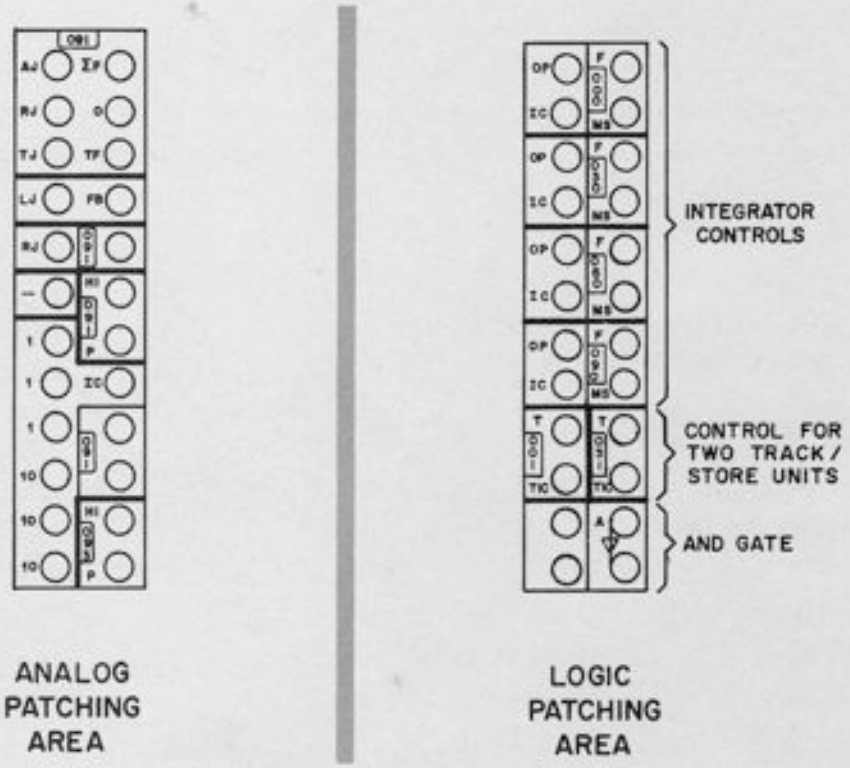


Figure 7.1. Patching Area for Track/Store Summer

The mode is determined by the "T" and "TIC" inputs on the logic panel. The "TIC" input is the "stronger"; when it is high (logic ONE) the unit is in the *IC* mode regardless of the state of the "T" input. When the "TIC" input is low (logic ZERO), then the "T" input assumes control; a

logic ONE at this input produces the *track* mode, and a logic ZERO produces the *store* mode. This information is summarized in the following table:

TIC Input	T Input	Mode
1	ANY	IC
0	1	Track
0	0	Store

7.1.3 Circuit Details

A simplified schematic of the track/store summer is given in Figure 7.2. Basically, the track/store network consists of a storage capacitor, two electronic switches (called the "TRACK GATE" and the "STORE GATE" in Figure 7.2), and an IC network. The rest of the circuit is a conventional summer circuit: an amplifier and a summing resistor network.

The state of the TRACK GATE, STORE GATE, and IC RELAY are determined by the "T" and "TIC" inputs on the logic panel. In the *track* mode, the TRACK GATE is conducting, connecting the TJ (TRACK JUNCTION) to the amplifier, and the STORE GATE grounds the capacitor. In the *store* mode, the STORE GATE connects the capacitor to the amplifier and the TRACK GATE grounds the TJ, which assures that any inputs patched to the resistor network have proper loading at all times. The IC RELAY is de-energized (i.e., in the position shown) in both modes.

The *IC* mode is like the *store* mode, except that the IC relay is energized, thus charging the storage capacitor to the appropriate IC value.

The ΣF (Summer Feedback) and the TF (Track/Store Feedback) terminals are patched to the amplifier output to make the unit a summer or a track/store unit. This connection is made by the bottle plug. Note that the bottle plug also connects RJ to TJ (Resistor Junction to Track Junction) for track/store operation, and RJ to AJ (Amplifier Junction) for use as a summer. Thus, when the unit is used as a summer, the track/store circuitry is completely removed from the circuit (note the normally-closed contact on the AJ terminal).

The resistor network may be borrowed for use with another amplifier if not needed for the track/store unit. Seven resistors are available, including the feedback resistor. Note that

the RJ is terminated *twice* on the patch panel, so that even if it is bottle-plugged to AJ or TJ it is still available for additional inputs.

NOTE

If the resistor network is borrowed for use with another amplifier, the operator must either use the ΣF terminal as a 100K input resistor or insert a pin in it; otherwise the network is normally connected to the IC network on the track/store summer. (See Figure 7.2.)

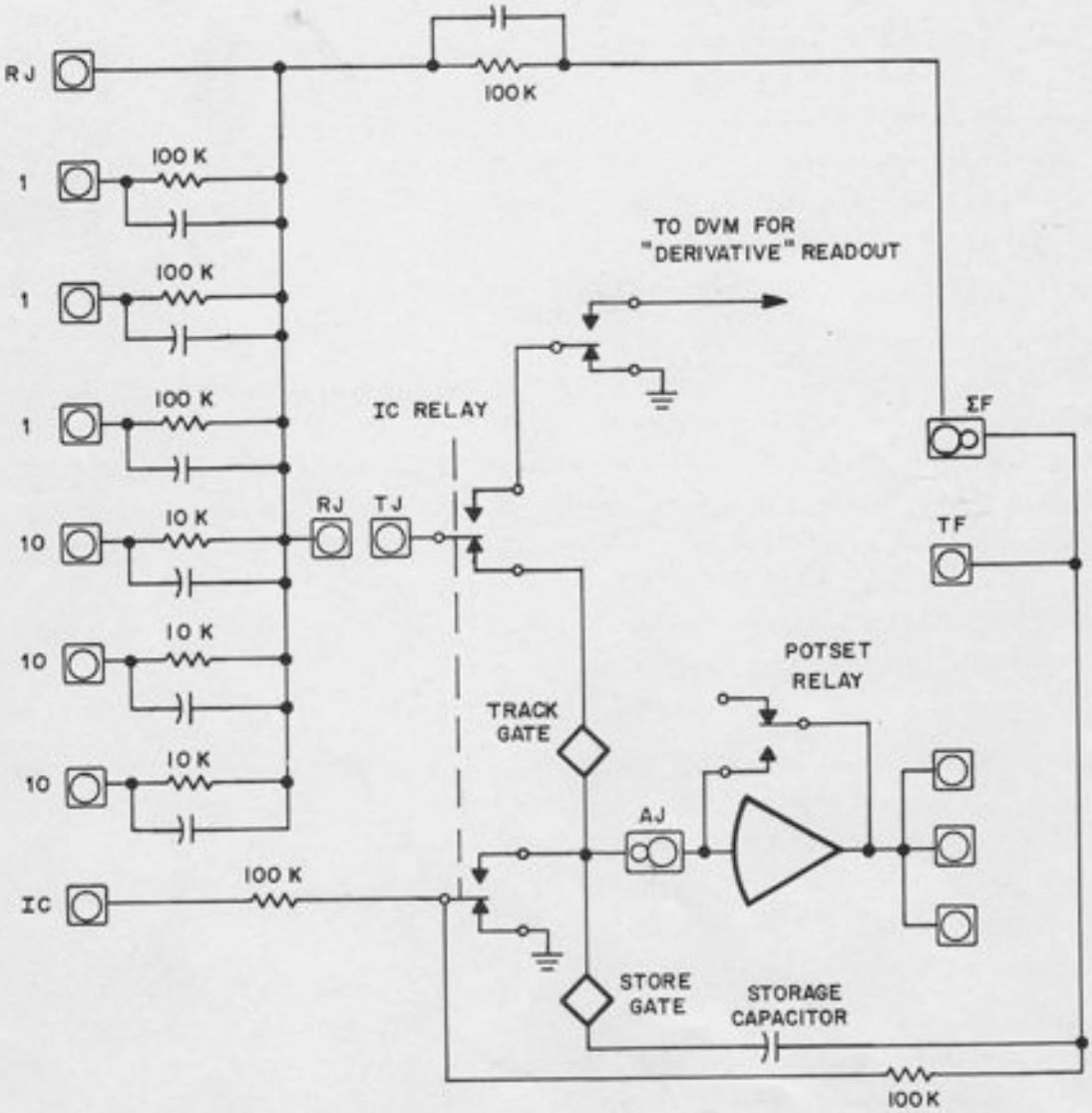


Figure 7.2. Simplified Schematic of Track/Store Summer

7.1.3.1 *Wide Range Feature.* The storage capacitor has a value of 0.003 microfarad when the unit is tracking giving an effective tracking lag of 300 nanoseconds. When the unit switches from *track* to *store,* a large capacitor (1.0 microfarad) is switched into the feedback path of the amplifier for long-term, low-drift storage. A 10-millisecond delay is included after the mode switches from *track* to *store* to allow the large capacitor to charge to the value stored by the small one. Thus there is no compromise between the small capacitor value needed for fast tracking and the large value needed for long-term low-drift storage.

7.1.3.2 *"Derivative" Readout.* When a track/store unit is in the *IC* mode (for example, during a static check) the output is determined by the IC input; the other inputs are disconnected. To assure that these inputs are being summed correctly, it is necessary to disconnect the TRACK JUNCTION from ground and connect it temporarily to the summing junction of the DVM. This is done through the readout system by addressing the "Derivative" (either D or D/10). The readout is electrically similar to the derivative readout on an integrator, but it is not a true derivative -- it is the sum of all the inputs to the TJ, *plus the output voltage* (since the feedback resistor is connected to the TJ).

7.2 THE LIMIT SUMMER

The limit summer (Figure 7.3), in addition to functioning as a regular summer, contains a zero-limit network which may be used to prevent the output from changing sign. A "+LIM" connection (double-vertical plug) limits the output to positive values; when the output "tries to become negative" it is held at zero. A "-LIM" patching connection (double-horizontal plug) limits the output to negative values. If nothing is patched into the terminals in the control area, the unit functions as an ordinary summer.

7.2.1 Location and Addressing

All amplifiers whose address ends in -6 are limit summers; thus there are a total of 12 summers with this feature. In addition certain JI's (Junction Inverters) have the same sort of limit network; see Paragraph 9.1.3.

7.2.2 Applications

7.2.2.1 *Regular Summer Applications.* To use the unit as a regular summer, omit all patching in the four terminal control areas. The limiting network has no effect, and the unit may be used as a summer, pot feedback amplifier, etc., in the usual way.

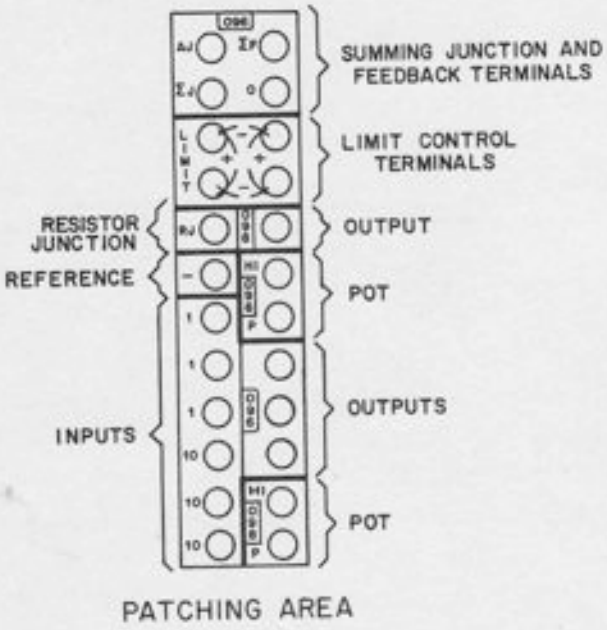


Figure 7.3. Patching Area for Limit Summer

7.2.2.2 *Absolute Value.* For an accurate absolute value, use the circuit in Figure 7.4a. When $x > 0$, the output of the amplifier with the limit connection is negative; hence the limit connection has no effect. The net input to the second amplifier is $-2x + x = -x$, and its output is $+x$. When $x < 0$, the limited amplifier would be positive, except for the limit connection which holds it at zero. Hence, the net input to the second amplifier is x, and the output is $-x$, which is positive. To generate $-|x|$, use a +LIM connection on the inverter. Note that the output amplifier does *not* have a LIM connection; it is a conventional summer.

7.2.2.3 *Dead Zone.* A dead-zone circuit is a circuit whose output is zero until the input exceeds a given value; beyond this point, the output increases linearly. The circuit in Figure 7.4b provides very sharp corners and accurate slopes. The ± boundaries of the dead zone may be set to different values if desired.

7.2.2.4 *Incompressible Spring.* In mechanical problems it is occasionally necessary to simulate a spring that can be stretched, but not compressed (for example, a cable exerts a force when under tension, but goes slack if its end points are closer together than its unstretched length). The cable thus exerts a force given by:

$$f = k(x_1 - x_2) \text{ if } x_1 > x_2$$

$$f = 0 \text{ if } x_1 < x_2$$

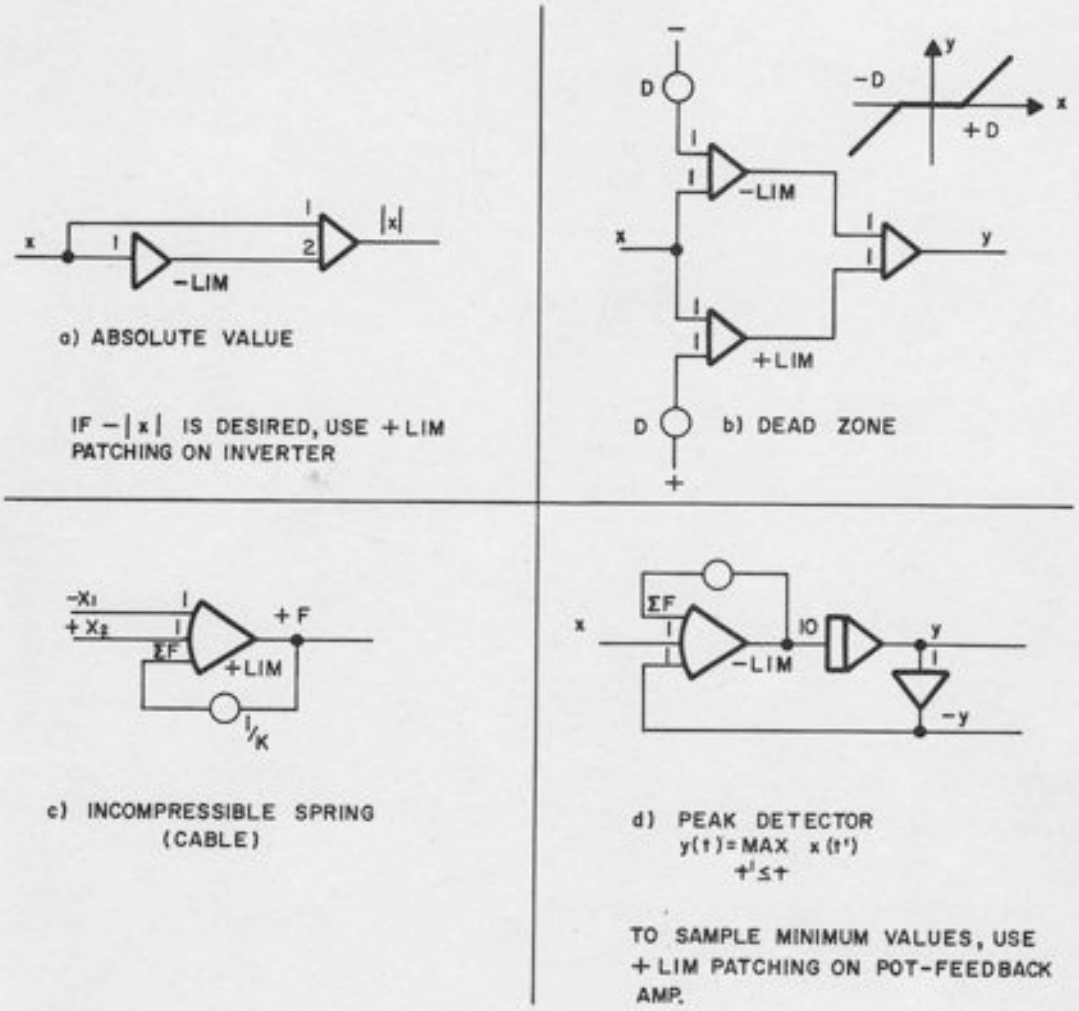


Figure 7.4. Typical Applications of the Limit Summer

The force may be easily generated by a zero-limit summer, as shown in Figure 7.4c. Note the use of pot-feedback for the factor K.

7.2.2.5 *Peak Detector.* To sample the maximum value of an input signal, the circuit of Figure 7.4d may be used. When $y - x > 0$, the output of the limited amplifier would be proportional to y-x, which is positive; the -LIM connection keeps this output at zero, and hence keeps y constant. When $y \leq x$, the output of this amplifier is negative, and hence the limit has no effect. Thus the value of y is allowed to change. The three amplifier loop has a short time-constant because of the high gain on the pot-feedback amplifier; hence it tracks x with only a small lag.

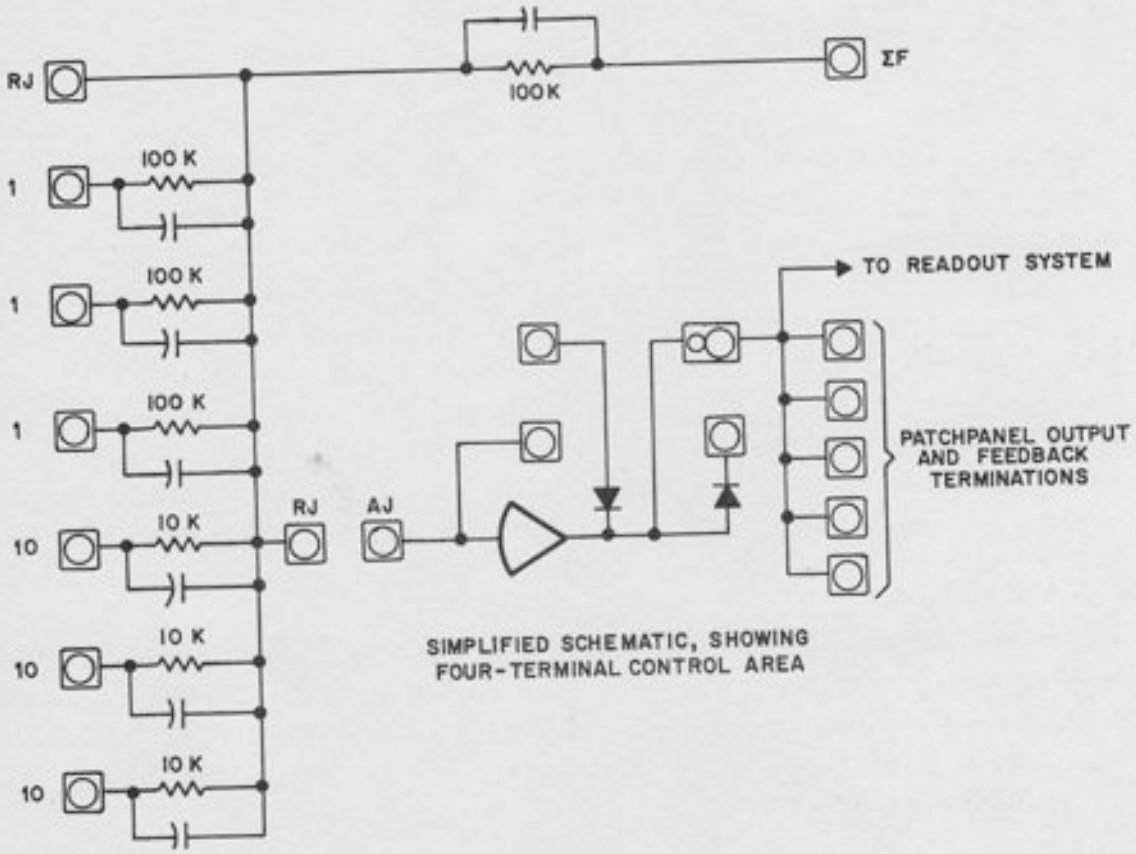


Figure 7.5. Simplified Schematic for Limit Summer

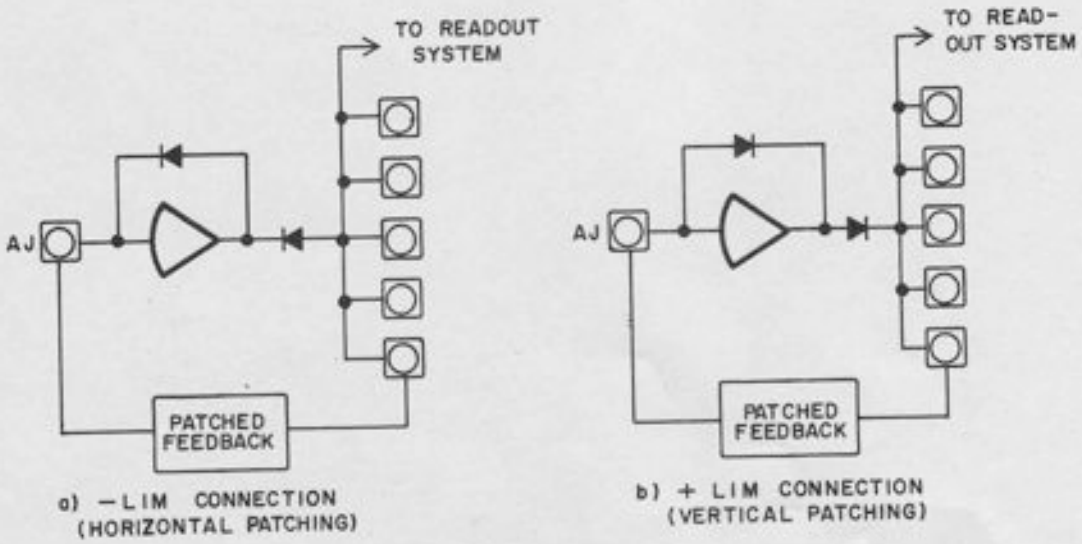


Figure 7.6. Equivalent Circuits of Limit Summer with Bottleplug Inserted

7.2.3 Circuit Details

Figure 7.5 shows the schematic for the limit summer. Note the normally-closed contact which connects the output of the amplifier to the readout system and to the patch panel. When nothing is patched into the four-terminal control area, the amplifier output is connected to the patch panel, and the two diodes have no effect. The conventional summer terminals (Amplifier Junction, Resistor Junction, output terminals, etc.) operate in the usual way.

When a plug is inserted in the control area, the circuit of Figure 7.6 results. For concreteness, only the +LIM case (Figure 7.6b) will be analyzed. Note that one of the diodes is actually in the feedback path. The output appearing on the patch panel is not the amplifier output, but comes from the other side of the diode. This diode performs the actual limiting operation, since it will not conduct when the amplifier output is negative. The other diode simply prevents overload by assuring that the amplifier has feedback, even when the output is negative.

For positive outputs, the amplifier behaves normally. Since the feedback connection is patched on the patch panel the diode characteristics do not affect the accuracy of the output at the patch panel. When the amplifier output becomes negative, the output at the patch panel becomes zero, since the output diode stops conducting. The other diode conducts, preventing the amplifier from overloading.

NOTE

Any type of resistive feedback may be used, including pot feedback. Similarly, the output may feed a number of pots and/or input resistors. However, the output should not feed non-linear loads (DFG's, multipliers, etc.), with the exception of the log/exponential DFG. If non-linear loads must be driven with this output, an additional inverter should be used as a buffer. The reason for this restriction is that the total current through the output diode must be zero when the output voltage is zero. This will be the case for any combination of resistive loads and resistive feedback, but will not be true for non-linear loads, since DFG inputs and multiplier inputs can draw current from their input terminals even when the input voltage is zero. The log/exponential DFG has been designed to draw no current from its input terminal when the input is zero; hence this DFG may be used in the feedback path of a limit summer. This feature is used in preventing zero crossover in the wide-range exponentials (see Appendix 5).

CHAPTER 8

THE POTENTIOMETER

A fully-expanded 680 has provision for 120 servo-set pots and 12 hand-set pots.

8.1 SERVO-SET POTS

8.1.1 Location and Addressing

The servo-set pots are numbered sequentially from P0 to P119. Twenty-four of these pots (those whose address ends in -4 or -9) are three-terminal pots; the remainder are two-terminal pots, with the lower end grounded. However, all three-terminal pots have their lower end *normally* grounded (through normally-closed patch panel switches). Hence, if nothing is patched into the lower terminal, a three-terminal pot behaves like a two-terminal pot, and may be patched, read out, and set like any other pot.

Five servo-set pots are terminated in each field, but not all pots are terminated in the tray with the same number. Figure 8.1 shows the pattern of pot locations; this pattern is the same for all fields. Note that each summer or integrator has two pots in the same tray. One of these pots has the same address as the amplifiers; the other has an address greater by two. Thus tray 90 contains P90 and P92; tray 91 contains P91 and P93. This arrangement associates the majority of the pots with the summers and integrators. Of course, they may be used with any amplifiers.

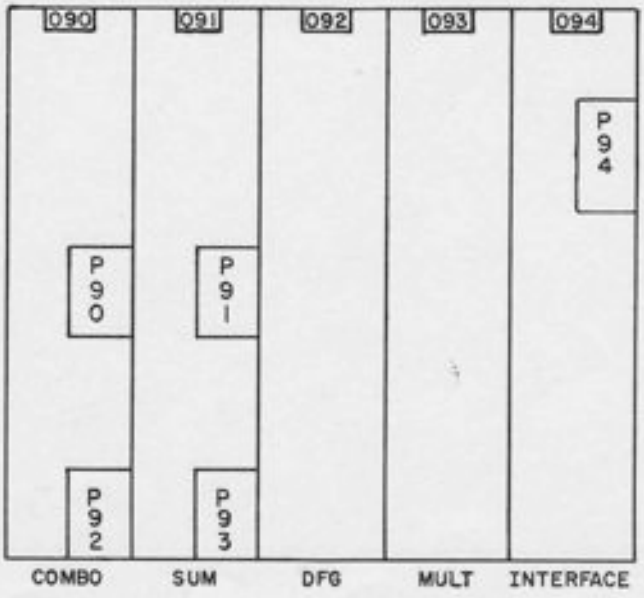


Figure 8.1. Servo-Set Pot Locations Within a Field

8.1.2 Normally-Closed Connections (Figure 8.2)

As mentioned in Paragraph 8.1.1, every three-terminal pot has its lower end grounded through a normally-closed set of patch panel contacts. Hence, the pot may be used as a regular two-terminal pot without the necessity of patching its lower end to ground. In addition, *every* pot (two-terminal or three-terminal) has its HI end normally connected to the amplifier terminated in the same tray. Thus the output of A90 is normally connected to P90 and P92. However, patching in any other input to the pot automatically disconnects the amplifier.

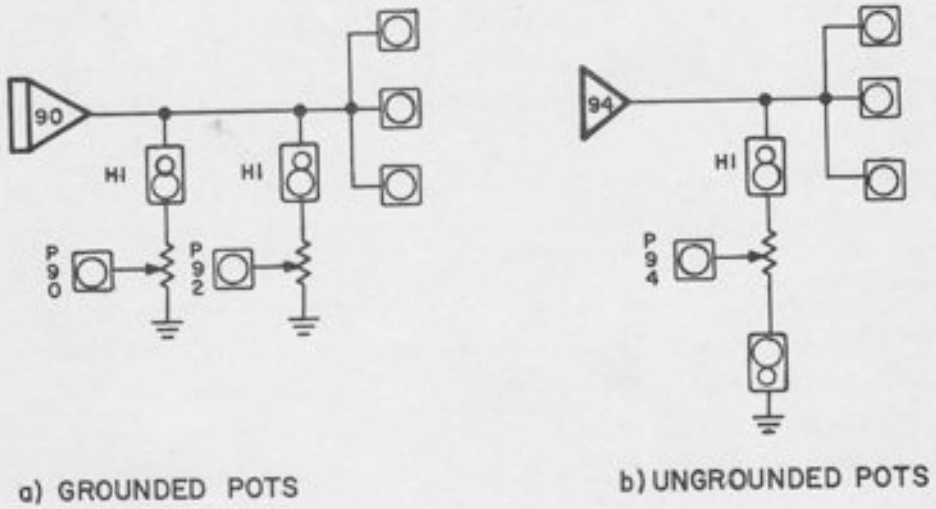


Figure 8.2. Normally-Closed Connections on Pots

8.1.3 Setting Procedure

The setting procedure for servo pots is covered in Chapter 4.

8.2 HANDSET POTS

The 680 has 12 handset pots, addressed with the letter Q. The pots are terminated in the "extra" COMBO trays in the top row (i.e., trays 2, 7, 12, 17, 22, and 27). There are two handset pots in each of these trays, which makes the patch panel area for these integrators identical with the corresponding area for the other integrators.

The handset pot address follows the rule for servo-set pots; each integrator tray with address N contains pots N and N+2. Hence, tray 2 contains Q2 and Q4, tray 7 contains Q7 and Q9, etc. Note that this leaves "gaps" in the sequence; there is no Q3, no Q6, etc. All handset pots have addresses N or N+2, where N is the address of one of the "extra" integrators in the top row.

Handset pots may be set in any mode. If it is desired to set them to a specific co-efficient, then the *PC* mode is recommended. The *SP* mode should *not* be used for these pots, because the GO key alternates the keyboard function between the *address* and *value* mode. Since no values are entered digitally for handset pots, the *PC* mode is used to allow the entry of addresses only.

The 12 handset pots are located in a strip between the analog and logic readout panels.

CHAPTER 9

FIXED DFG'S AND JUNCTION INVERTERS

In addition to the variable DFG terminations, (see Chapter 10) each DFG tray contains two other major components: a fixed DFG and a junction inverter (JI for short). Unlike the variable DFG, the fixed DFG and the JI are located in the tray itself.

Two types of fixed DFG units are currently available; the sine/cosine unit and the dual log/exponential unit. The sine/cosine unit generates the sine *or* the cosine of an input θ; the dual log/exponential unit allows *two* independent natural log or exponential functions to be generated. There are also fixed squaring DFG's in the multiplier; see Chapter 11 for details.

Although the JI and the DFG may be used completely independently, they are closely associated, and hence are described in the same chapter.

9.1 THE JUNCTION INVERTER

The junction inverter (Figure 9.1) is an inverter whose summing junction appears on the patch panel. It is intended for two principal uses; as an inverter, and as an output amplifier for a fixed DFG. The DFG and JI in the same tray bear the same address, and are arranged for easy bottle-plug patching. Hence, when the JI is used as the output amplifier for the DFG, they may be thought of as the same component, and represented in circuit diagrams by a single symbol.

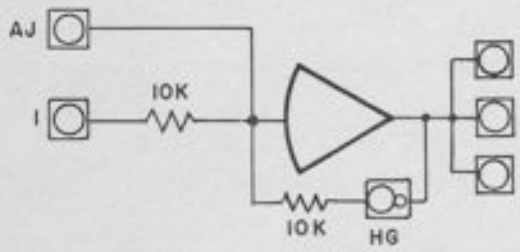


Figure 9.1. Simplified Schematic, Junction Inverter

9.1.1 Location and Addressing

Since each DFG tray contains a JI, all amplifiers ending in -2 and -7, from 32 to 117 are JI's, a total of 18 JI's in DFG trays. In addition, each interface tray contains a JI, whose address ends in -4 or -9. Since there are 24 interface trays, there are 24 such JI's, which gives a

total of 42 Junction Inverters in the entire computer. All JI's, regardless of location, are identical, with the exception of the zero limit feature discussed in Paragraph 9.1.3.

9.1.2 Applications (Figure 9.2)

As mentioned above, the principal uses of the JI are as an output amplifier for fixed DFG's, and as an inverter. Patching instructions are given below; explicit patching diagrams and symbols are given in Appendix 1.

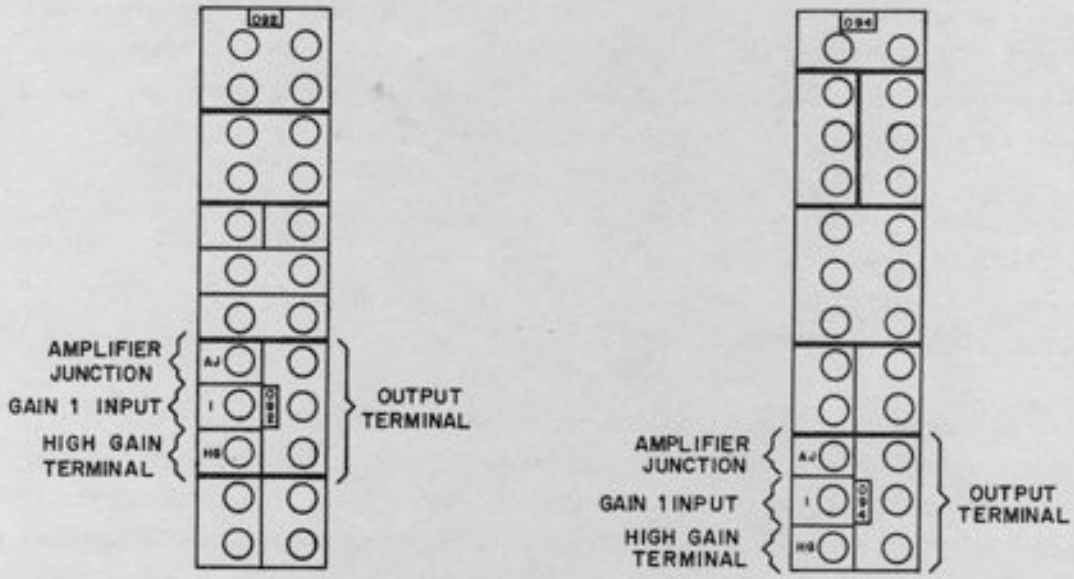


Figure 9.2. Junction Inverter Patching Areas

9.1.2.1 *Use as Inverter.* To use the JI as an inverter, simply patch x into the "gain 1" input terminal. The output -x appears at the output terminals. The input and feedback resistors are 10K each.

9.1.2.2 *Use as DFG Output (Figure 9.3).* The JI is arranged for convenient use as the output amplifier for a fixed DFG; it may be bottle-plugged to the associated FDFG or connected to any other FDFG by patchcord. Since the JI has its own feedback resistor, only one patching connection (the junction connection) is required to connect it to any FDFG designed for use with a 10K feedback; this includes the log/exponential DFG, the multiplier, and the x^2 DFG (which is one-half of a multiplier - see Chapter 11). Connection to a sine/cosine DFG requires removal of this 10K resistor, since the sine/cosine DFG uses a non-linear feedback network instead. For further information, see Paragraphs 9.2 and 9.3, and Appendix 1,

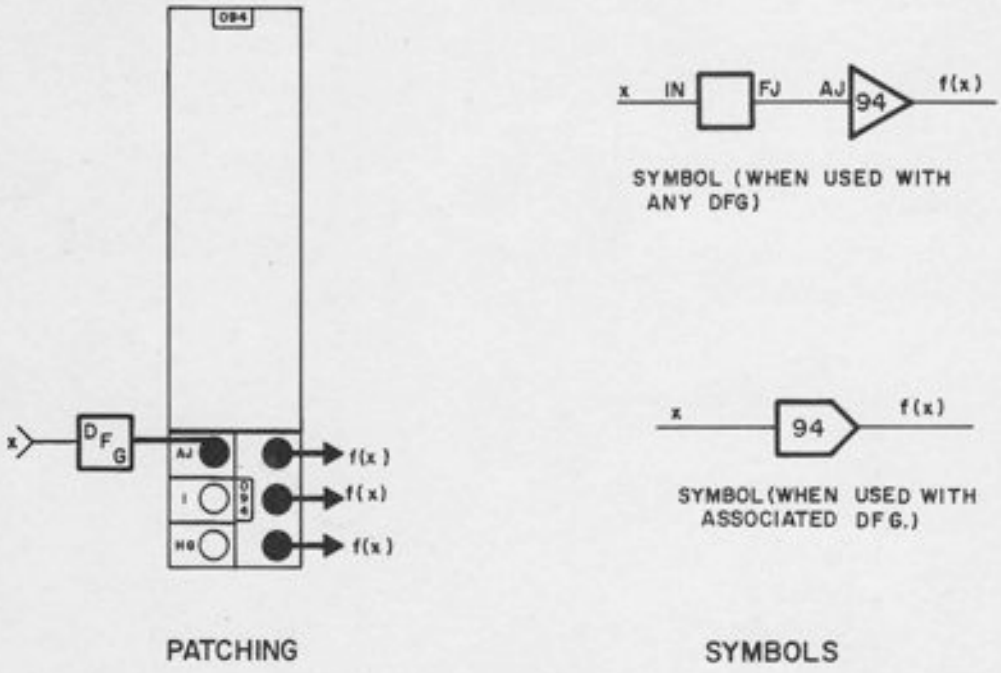


Figure 9.3. Use of the Junction Inverter as a DFG Output Amplifier

9.1.2.3 *Use as a High-Gain Amplifier.* To make the JI function as a high-gain amplifier, all that is required is a pin in the terminal marked "HG". This pin disconnects the normally-connected feedback resistor and allows arbitrary feedback connections to be externally patched.

9.1.2.4 *Use as a Summer.* The JI may be used as a summer by patching additional resistors to the AJ (amplifier junction); however, such use is rare, since it is easier to use the regular summers (see Chapter 7). Note that the feedback resistor is 10K; this fact must be taken into account when using external resistors.

9.1.3 Zero Limiting

Some of the JI's have a built-in zero limit network that permits accurate generation of absolute values, dead zone functions, and similar applications. This network is included only in JI's located in log/exponential DFG trays. The JI's in interface trays and in sine/cosine trays do not have this feature. A schematic is given in Figure 9.4. Applications are essentially those of the regular limit summer (see Paragraph 7.2). In addition, the zero limit is especially useful in preventing zero crossover in exponential circuits and several other circuits involving the log/exponential DFG; this is the reason for including the feature only in log/exponential trays. Details of this application are given in Appendix 5.

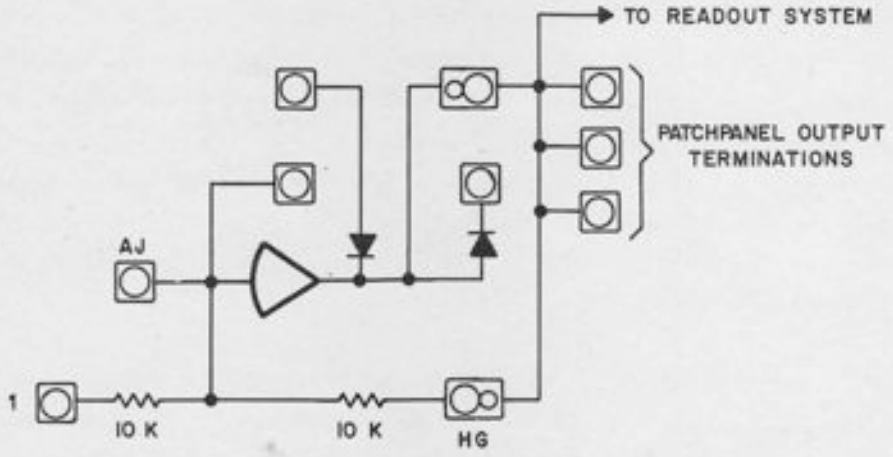


Figure 9.4. Simplified Schematic, Junction Inverter with Zero Limiting

9.1.4 Circuit Details

Schematics for the JI are given in Figures 9.1 and 9.4. Note the normally-connected feedback resistor, which permits use as an inverter by merely patching the input to the "1" terminal. To use the JI as an output amplifier for a non-linear element that requires a 10K feedback, one merely patches the current output ("Function Junction") of the DFG to the AJ ("Amplifier Junction"). In inverse operations (e.g., exponentials, square roots, division) the 10K resistor is used as the input element, and the DFG itself is in the feedback path; for such applications, the "HG" terminal may be used for the input, in which case, the "feedback" resistor becomes an input resistor. Standard modes of operation with FDFG's are described in Appendix 1.

For high-gain applications, a pin in the "HG" terminal disconnects the feedback resistor. If no pin is available, a vertical bottle plug connecting this terminal to the "gain 1" input above it will perform the same function.

The zero-limit JI combines the features of a regular JI with those of a limit summer. A more detailed explanation of the limiting principle is given in Paragraph 7.2.3. The notation "+Lim" underneath such an amplifier indicates that the output is limited to positive values, and vice-versa for "-Lim".

9.2 THE LOG/EXPONENTIAL DFG

9.2.1 Location and Addressing

Every one of the 18 DFG trays (the trays ending in -2 or -7 from 32 to 117) can contain a dual log/exponential DFG capable of generating two independent natural logs or exponential

functions. These same trays can also contain other types of fixed DFG's, such as the sine/cosine DFG described in Paragraph 9.3. The standard 680 configuration has log/exponential DFG's only in the second analog row (trays 32, 37, 42, 47, 52, and 57). The 12 DFG trays in the lower two rows contain sine/cos DFG's. However, a log/exponential tray may be used in any DFG position. If it is used in one of the lower rows, an overlay should be used on the patch panel to make the patching terminations consistent.

9.2.2 Patch Panel Terminations

The patch panel terminations for a dual log/exponential DFG are given in Figure 9.5. Note that each DFG has an input terminal (marked "IN" and an output terminal marked "FJ" Function Junction). This is the terminal that should be connected to the Amplifier Junction of the appropriate output amplifier. Any of the 120 amplifiers whose AJ appears on the patch panel may be used. The unit is intended normally to be used with the JI immediately beneath it; however, this is not always possible, since each log/exponential tray contains two DFG's and only one JI. When another output amplifier must be used, it is preferable to pick one with a regular 10K feedback resistor, such as a JI in another tray, or the output amplifier of a quarter-square multiplier, if the multiplier is not in use.

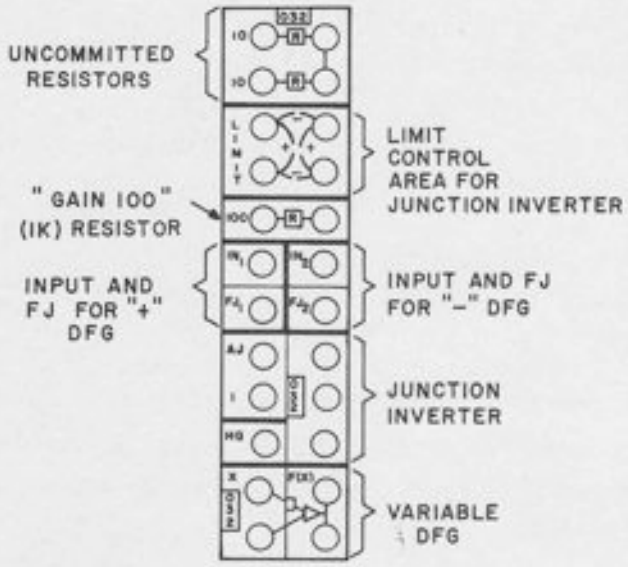


Figure 9.5. The Log/Exponential DFG Patching Terminations

In addition to the JI and the log/exponential DFG, the tray contains ± LIM connections for the JI, (Paragraph 9.1) and an uncommitted 1K resistor (Gain "100" - see Paragraph 12.3). The vari-

able DFG at the bottom of the tray (see Chapter 10) and the uncommitted "Gain 10" resistors (10K) at the top of the tray are common to *all* DFG trays, including the sine/cos tray.

9.2.3 Basic Input/Output Relation

When the + type log/exponential DFG is used as the input element to an amplifier with a 10K resistor, the input/output relation becomes:

$$y = -\frac{1}{10} \log x$$

The word "log" means "natural log." A circuit for obtaining base 10 logs is given in Appendix 5.

If the DFG is used as the feedback element, with a 10K resistor as the input element, the exponential (inverse) relation is obtained. Solving the above relation for x in terms of y, the inverse relation becomes:

$$x = e^{-10y}$$

In these equations, x and y are given in machine units (one unit = ten volts); hence, both x and y may range from 0 to 1.0.

Table 9.1 illustrates the input/output relation.

Table 9.1

Y	0.0000	0.1000	0.2000	0.3000	0.4000	0.5000	0.6000	0.7000	0.8000	0.9000	1.0000
X	1.0000	0.3679	0.1353	0.0498	0.0183	0.0067	0.0025	0.0009	0.0003	0.0001	0.000045

Note that as the input varies from 0 to 1.0, the output varies from unity down to a very low value (in fact, rounded off to four decimal places, the value 0.000045 becomes 0.0000). Thus the exponential function is generated over a range of e^{10}, or 20,000 to 1, which is consistent with the resolution of the rest of the analog components.

By simply increasing the amplifier gain, exponential functions with a wider range (e.g., 7 or 8 decades) may be easily generated. However, whenever the *theoretical* output is less than about 1/20,000 of its maximum value the *calculated* output is zero. Examples of "wide range" variables are discussed in detail in Appendix 4.

If input and output are measured in volts instead of units, then the equation becomes:

$$y = -\log(x/10)$$

$$x = 10e^{-y}$$

The appropriate range becomes from 0 to 10, and the numerical entries in Table 9.1 should be multiplied by 10.

The input/output relation of the -DFG is the same as for the +DFG, except that the input and output polarities are reversed; the output is given by:

$$y = +\frac{1}{10} \log(-x)$$

and both x and y are negative.

9.2.4 Circuit Details

The basic log generator is a two-terminal device from the programmer's point of view. The IN terminal accepts an input voltage (which must come from an amplifier, not a pot, because it presents a non-linear load). The FJ (Function Junction) is the output terminal which should be connected to virtual ground (an amplifier junction). It delivers into this junction a current proportional to the log of the input and hence may be regarded as a non-linear resistor.

When the unit is used in the feedback path of a high-gain amplifier, the result is an exponential function. The input is through a 10K resistor (or other resistor value if "wide-range" exponentials are desired). This input may be attenuated with a pot, since its load is linear. When the DFG is used with an arbitrary amplifier, the DFG and the amplifier should be considered as separate components and drawn accordingly. When used with the associated amplifier, the two symbols may be "blended" into one, indicating that the DFG and amplifier are considered as a single component. (See Figure 9.3, and Appendix 4.)

9.3 THE SIN/COS DFG

Each sin/cos DFG is capable of generating either the sine *or* the cosine of an input variable. The input variable may range over one complete revolution (±180°).

9.3.1 Location and Addressing

All 18 DFG trays (trays ending in -2 or -7 from 32 to 117 inclusive) may contain sin/cos DFG's. However, in the standard configuration, only the lower two rows (trays 62 to 117 inclusive)

contain sin/cos DFG's (a total of 12), and the others contain log/exponential DFG's. If sin/cos DFG's are put in the other trays (32 through 57) an overlay should be used on the patch panel to make the patching terminations consistent.

9.3.2 Patching Terminations

The patching terminations for the sine/cosine generator are shown in Figure 9.6. Although the detailed patching diagrams are given in Appendix 1, the following brief description of the functions of the terminals is given here:

9.3.2.1 *The θ Input.* This is the input terminal. It accepts the input θ, which must be scaled as (θ/200) (on a unit scaled basis) or θ/20 in volts. The maximum allowable value of θ is ±180° = 0.9000 units or 9.000 volts.

9.3.2.2 *The "C" Input.* This is the control input - it allows the operator to determine the output function generated. When C is left unpatched, the output is -sin θ. Patching "C" to +Reference produces -cos θ, and patching "C" to -Reference produces +cos θ.

9.3.2.3 *The "J" and "F" Terminals.* These terminals (Junction and Feedback) are to be connected to the amplifier junction and the output of an externally patched high-gain amplifier. The output of this amplifier, called the "shaping amplifier", is not normally of interest to the programmer; it is rarely useful for anything except to serve as part of the sine or cosine circuit. Hence, it is *not* generally recommended that the amplifier in the same tray be used; this amplifier should be saved for the output amplifier. The shaping amplifier may be any high-gain amplifier, such as a JI with a pin in the "HG" terminal.

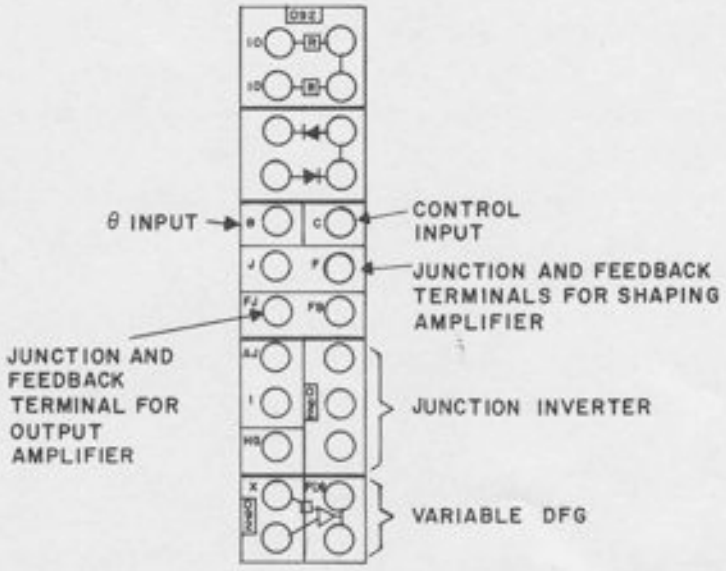


Figure 9.6. Patching Terminations for Sin/Cos DFG

9.3.2.4 *FJ and FB.* These terminals (Function Junction and Feedback) are to be connected to the AJ and output, respectively, of a high-gain amplifier. This amplifier serves as the output amplifier for the DFG; the output -sin θ or $\pm\cos\theta$ appears at its output terminals. It is recommended that the associated JI be used; it is in the same tray immediately below, has the same address, and may be easily connected by bottle-plug. Note that a pin in the "HG" terminal is necessary.

9.3.3 Circuit Details

The sin/cos DFG differs from other DFG's in that, for normal use, it uses non-linear networks both in the input *and* in the feedback of a high-gain amplifier. The main non-linear network is in the feedback path; this network contains the segments necessary to generate the sine function over the interval $-90° \leq \theta \leq +90°$. The input network, or shaping network, operates in conjunction with the externally-patched shaping amplifier to extend the range to $\pm 180°$. This is accomplished by biasing and switching the input so that the same feedback network is used twice. A detailed schematic is not included here; see the maintenance manual for more specific information.

The "C" terminal operates by biasing the input, thus "phase shifting" the output. In other words, it makes use of the identity:

$$\sin(\theta \pm 90°) = \pm \cos\theta.$$

Connecting the control input to ±Reference produces a bias into the unit through an appropriate resistor which is equivalent to shifting θ by 90°.

Under some conditions, the shaping amplifier may be omitted. For example, -sin θ may be generated over the restricted range $-90° \leq \theta \leq +90°$ without patching the shaping amplifier; this circuit and others mentioned in this chapter are detailed in Appendix 1.

Finally, interchanging the input and feedback connections allows the generation of the inverse functions arc sin x and arc cos x; patching and symbols are given in Appendix 1.

CHAPTER 10

THE VARIABLE DFG

The variable DFG allows the generation of arbitrary continuous nonlinear functions by means of straight-line-segment approximation. Both ten-segment and twenty-segment operation are possible.

10.1 LOCATION AND ADDRESSING

A fully-expanded 680 contains 18 ten-segment DFG's. Their addresses end in -2 or -7, and run from 32 to 117 inclusive. The DFG's are arranged in pairs, and each pair may be used as a twenty-segment DFG or as two ten-segment DFG's. The DFG's themselves are located in slideout drawers to the right of the operator.

The two DFG's in a pair have identical addresses except for the last digit; thus F32 and F37 form one pair, F42 and F47 form another, and so on. In a 20-segment operation, the *first* DFG (the one ending in -2) uses all 20 segments; the output amplifier of the second DFG is available as an inverter. In a standard computer configuration, the first DFG in a pair is a +DFG, capable of accepting positive inputs, and the second one (the one ending in -7) is a -DFG, which accepts negative inputs. Either type of DFG can produce either positive or negative *outputs*. Figure 10.1 shows the patching area for the VDFG terminated at tray 92.

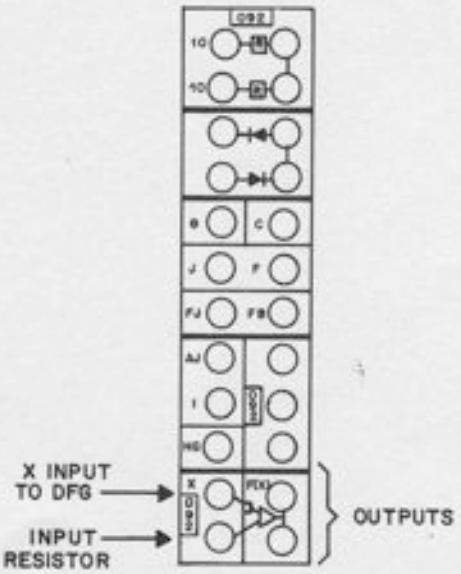


Figure 10.1. Variable DFG Patching Terminations

10.2 APPLICATIONS

The main application for a DFG, of course, is function generation; however, the inclusion of an additional input resistor for each DFG allows some alternative applications such as the use of the unused output amplifier as an inverter, and combined summation and function generation. Symbols and patching for these modes of operation are given in Appendix 1; circuit details are given in this chapter, in Paragraph 10.4.2.

10.3 SETUP PROCEDURE

Since the diode function generator approximates a given curve by a series of straight-line segments, the first step in the setup of any DFG is to determine the location of the breakpoints ("corners") in order to fit the curve as smoothly as possible. Usually the desired curve is given in graphical form, and the programmer must determine, by inspection of the graph, a table of values of x and f(x) for setup. Sometimes the function is given in tabular form - a table of values of x and f(x). Such a table of values is usually the result of experimental measurements, although it may represent the result of a series of calculations.

If the function is given in tabular form it is tempting to simply set up the DFG to the values of x and f(x) from the table, especially if the number of data points in the table happens to coincide with the number of segments available in the DFG. The difficulty with this approach is that the distribution of the data points that define the function will probably not be the best distribution of breakpoints for straight-line approximation. For example, the original data may have been obtained for equally-spaced values of the input variable x, whereas it is generally *not* a good idea to use equally-spaced breakpoints for segment approximation. It is better to plot the data points, pass a smooth curve through them, and determine a good breakpoint location from this smooth graph. In any case, it is desirable to know "what the function looks like" before trying to set it up, which means it should be plotted before set up.

Hence, set up procedure in this chapter assumes from the start that the function is defined graphically. The procedure will consist of determining good breakpoint locations, tabulating the values of x and f(x) at these points, and setting up the function from this table of values. The 680 DFG's have a setup panel that permits the direct setup of values of x and f(x); both the input x and output f(x) may be read directly on the DVM during setup.

An alternative procedure, illustrated in Paragraph 10.3.4, skips the table and consists of setting up the function on an X-Y plotter. The procedure is exactly the same, as far as "button-pushing and knob-twisting" are concerned, but the operator looks at the plotter, instead of the DVM.

In any case, even if the function is set up from a table of discrete values read out on the DVM, it is a good idea to obtain a continuous plot of f(x) versus x to make sure that the function has been set up correctly. Such a plot should be a part of the problem documentation, along with the circuit diagram, listings of pot-settings, assignment sheets, and so on. The 680 setup panel includes an integrator capable of generating a ramp input to the DFG for convenient plotting *without* patching changes. In fact, the DFG can be completely set up and the resulting curve plotted with the patch panel off.

10.3.1 Breakpoint Location

Given a smooth curve, where should the breakpoints be located to approximate it with minimum error? Although there exist analytical methods for dealing with this problem, they generally require too much computation to be of practical use. With a bit of experience, a good programmer can come very close to the optimum breakpoint location simply by inspection of the curve. The following general rules may serve as a rough guide to the techniques:

10.3.1.1 Keep in mind the total number of breakpoints available on the DFG. Most functions of practical interest may be adequately represented with 10 segments; a few require 20 segments. Most computers (including the 680) have ten-segment DFG's capable of being "paired" to handle the occasional twenty-segment function.

10.3.1.2 Start out by locating the areas where the function is nearly straight; the individual segments in such areas may be relatively long. In between these areas will be the areas of rapid slope-change; the breakpoints should be concentrated here.

10.3.1.3 As a general rule, it does not pay to locate two breakpoints closer together than about 4% of full scale (i.e., 0.04 unit, or 0.4 volt on a ten-volt computer). If two breakpoints are spaced more closely than this, they tend to "blend" into one because of the characteristics of diodes, which are not perfect switches. This effect, which "rounds off the corners" of the function, gives a smoother output, and hence is beneficial, provided you know about it and take advantage of it in determining breakpoint locations. In case of very sharply curved functions, it may be necessary to space breakpoints slightly closer - say, as close as 2% of full scale (0.02 unit).

As an example, consider Figure 10.2. This curve represents an arbitrary function, scaled on a unit basis, so that both input x and output f(x) vary from zero to unity. The procedure starts by noting the two areas where the function is almost straight, namely $0 \leq x \leq 0.2$ and $0.6 \leq x \leq 0.8$. There would be little point in putting any breakpoints here, so the process starts by drawing two fairly long segments to approximate the function over these intervals.

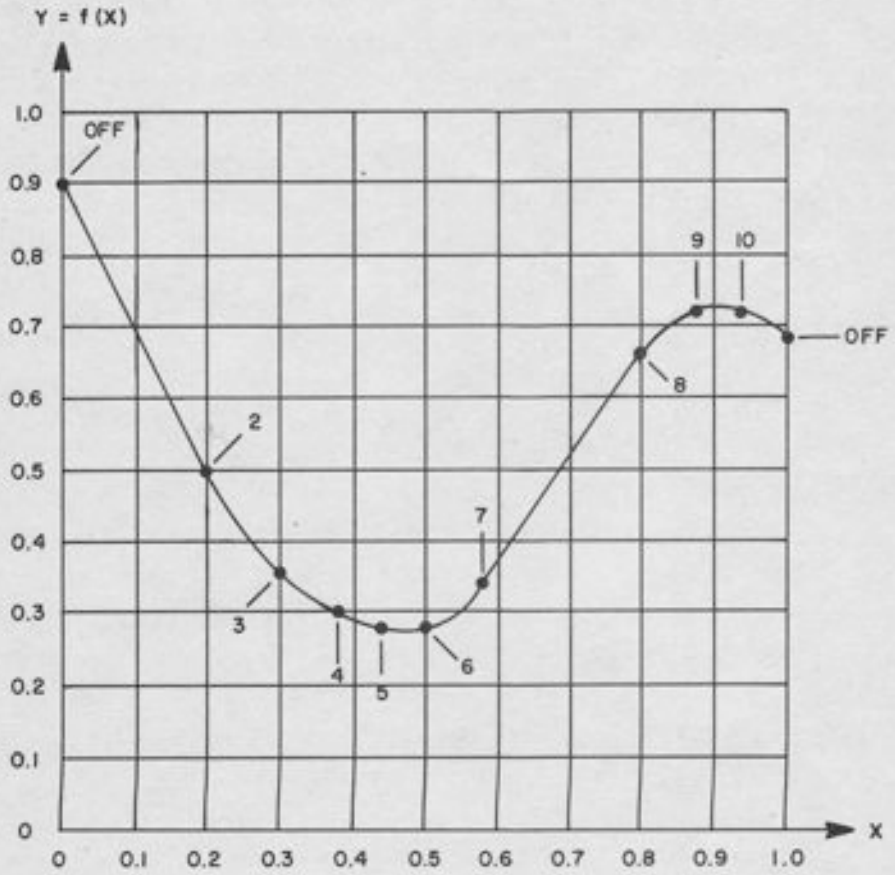


Figure 10.2. Typical Ten-Segment Function

The intervals from 0.2 to 0.6 and from 0.8 to 1.0 are the intervals where the function curves noticeably. Since this is a relatively "mild" function, it may be easily approximated by ten segments. Hence, there are *nine* breakpoints to be determined. (Note that the number of breakpoints is one less than the number of segments. For example, a two-segment function would have one breakpoint - where the two segments joined; a three-segment function would have two breakpoints, and so on. The *endpoints* of the interval are fixed, and are not counted as breakpoints.)

We have nine breakpoints to divide between the two intervals of rapid slope-change. Since the first interval is longer, and the slope changes somewhat more in this interval, more breakpoints should be put in this interval. A 6-3 split was decided upon, somewhat arbitrarily. A good case could also have been made for a 5-4 split; the decision is not critical.

Based on the 6-3 split, the breakpoint location in Figure 10.2 was determined. No claim is made that it is the absolute optimum, but it is a fairly good fit, and easily arrived at. In using the visual technique, there is no substitute for experience; the above rules and example are intended only as a rough guide.

10.3.2 DFG Setup Theory

In order to understand the DFG setup procedure, one particular aspect of the electrical theory of DFG's should be explained. Note that this knowledge is not, strictly speaking, necessary to *follow* the procedure, but only to *understand* it. However, mistakes are less likely to occur if the operator knows something about *why* various steps are taken; hence, this summary.

Each breakpoint, or "corner" in a DFG curve represents a diode that is changing state; as the input voltage moves away from the origin, in either the positive or the negative direction, more and more diodes start to conduct. Each diode, when it starts to conduct, increases or decreases the slope of the curve. The change in slope for a given segment is determined by adjusting a potentiometer (the slope pot). The change in slope introduced at a given point has no affect on the value of the function at that point, but does affect the value at subsequent points. For example, see Figure 10.3, which shows the affect of changing the slope pot for segment 5 on a partially setup function. The incremental slope introduced at x_5 does not affect the function value at that point, but does affect the value at the next breakpoint x_6. The tangent line represents the output with the SLOPE switch OFF.

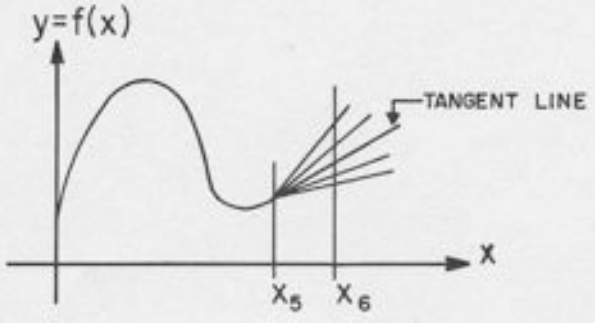


Figure 10.3. Effect of Changing Slope Pot 5 on DFG Output

The DFG setup procedure is arranged so that the operator does not observe slopes, but rather values of x and f(x). Hence, the function value at the sixth breakpoint is adjusted by means of the slope pot at the *fifth* and similarly for the other breakpoints. This fact is the key to understanding the setup procedure.

In practice, the slope pot for a given segment *does* have an effect on the value of the function at that point, due to the fact that the diode is not a perfect switch. The "corner" at x_5 in Figure 10.3 is somewhat rounded, and a slight shift in $f(x_5)$ will occur when setting $f(x_6)$. In many cases, this shift is negligible, but in a few cases, it necessitates a later "trimming" adjustment.

10.3.3 Setting a Ten-Segment Function

Once the values of x and f(x) are tabulated, the function setup is quite straightforward. The 680 variable DFG has potentiometers for adjusting slope and breakpoint for each segment. The DFG setup panel allows direct setting from a table of values; first adjust the breakpoint x (which may be read directly on the DVM), and then press a switch and set f(x).

As an example, consider the function in Table 10.1. This is the same function that was given graphically in Figure 10.2. Note that since *10* segments are to be used, the function is tabulated at *11* points, including the *2* endpoints and *9* breakpoints. A "+" DFG is assumed, and the endpoints are fixed at 0 and 1.

Table 10.1

x	y = f(x)
0.00	0.90
0.20	0.50
0.30	0.36
0.38	0.30
0.44	0.28
0.50	0.28
0.58	0.34
0.80	0.66
0.88	0.72
0.94	0.72
1.00	0.68

In setting such a function, most people will find it easiest to set all breakpoints (x values) first, and then, set the function values f(x). However, it is also possible to set the first breakpoint x, then set the corresponding f(x), and continue alternating in this manner. In either case, the procedure for setting a slope or a breakpoint is the same. The procedure makes use of the DVM and signal selector, and the setup panel (Figure 10.4), which is in the right half of the second drawer from the top (the first DFG drawer). The unit is marked "TIME BASE AND MDFG INPUT."

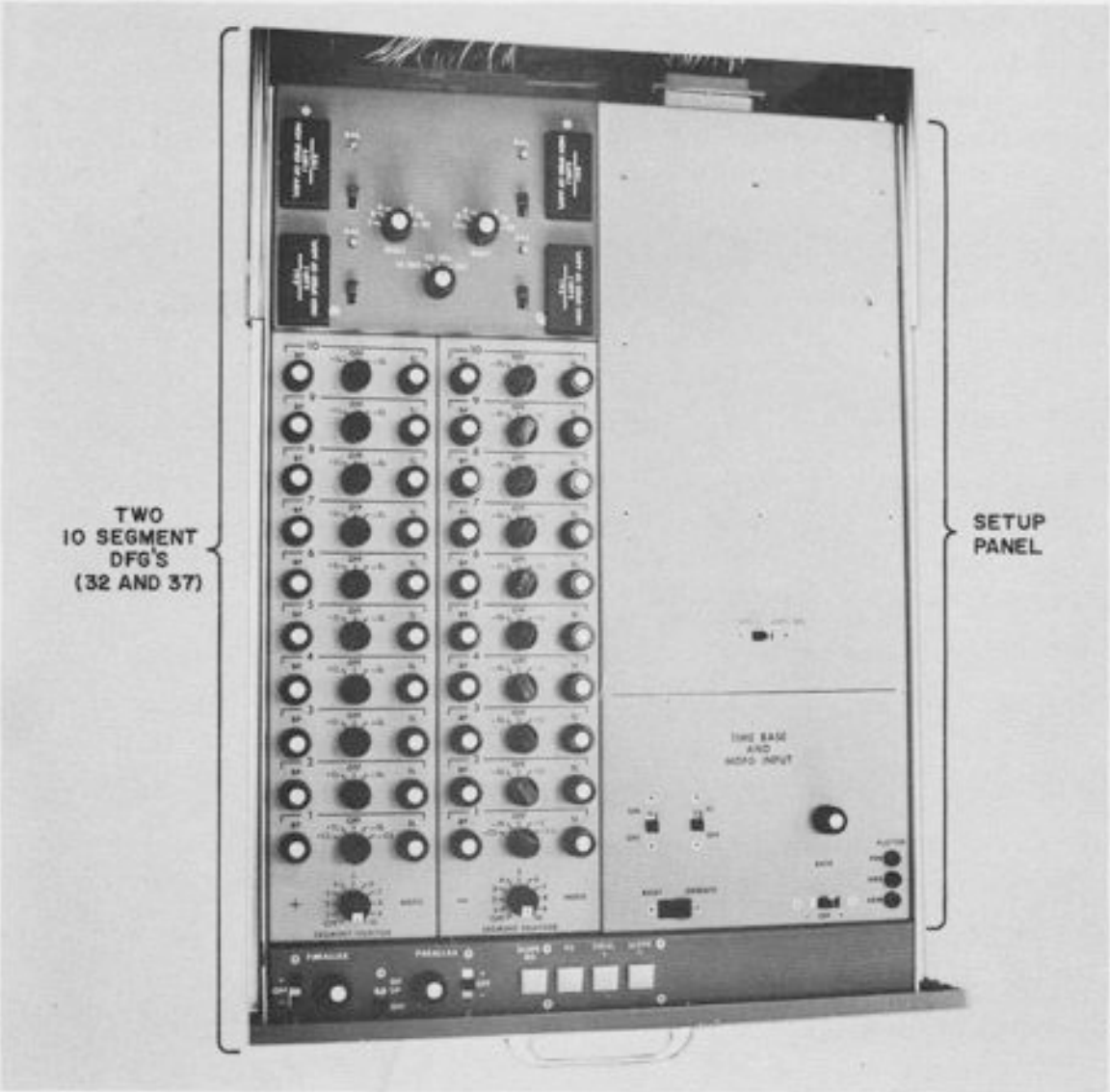


Figure 10.4. DFG Setup Panel (In Upper DFG Drawer)

10.3.3.1 *Computer Mode.* Select the *PC* mode. Although the unit may be set up in any mode, the *PC* mode prevents overloads of other components during setup. No patch panel need be inserted; however, if there is one on the computer, it does no harm.

10.3.3.2 *Setup Panel Switches.* Open the drawer containing the setup panel, and make sure that all switches are in the OFF position; this includes the switches marked "AMPL BAL", ON/OFF", "IC/OFF", and RATE. The switch marked RESET/OPERATE should be in the RESET position. Close the drawer.

10.3.3.3 *Selecting the DFG.* Address the DFG to be set on the signal selector. Its output should be near zero, since the computer is in the *PC* mode. Now open the drawer containing the DFG (Figure 10.5), and turn on the SETUP switch near the front of the drawer. There is one switch for each *pair* of ten-segment DFG's. When the SETUP switch for any DFG is turned on, the "F" button on the signal selector keyboard will light up. This button is also lit whenever the AMPL BAL switch is in the ON position. Hence, after setting up DFG's or balancing DFG amplifiers, the operator has a visual warning reminding him to turn off the setup panel before proceeding with computation.

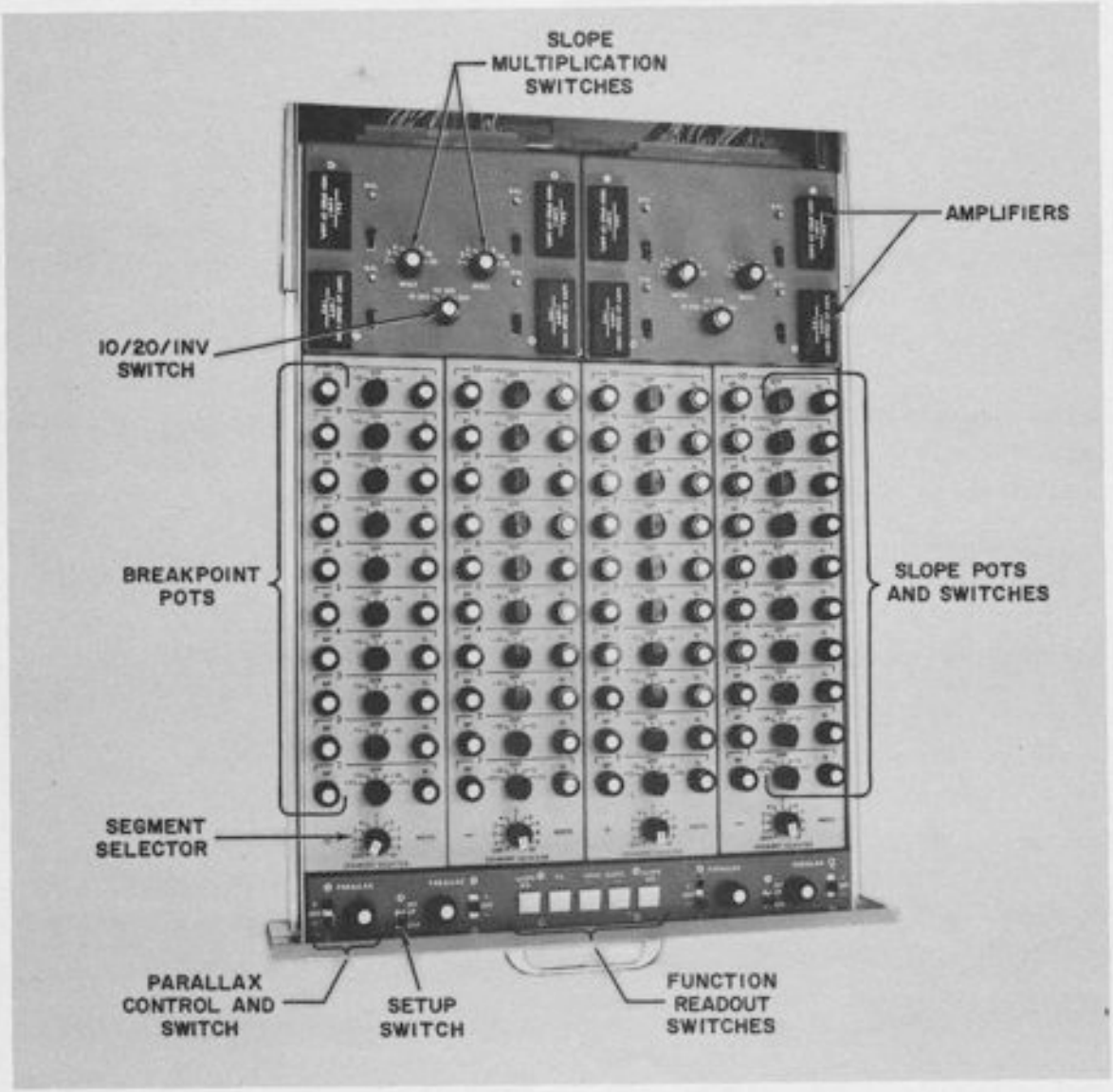


Figure 10.5. Typical DFG Drawer (Except for Upper Drawer)

10.3.3.4 *Checking other DFG's.* The operator should now check all other DFG's to make sure that their setup switches *and* their SEGMENT SELECTOR switches are all in the OFF position. Only one DFG can be set up at a time, and if several are turned on at once, they will be interconnected through the setup panel, making accurate setup impossible.

10.3.3.5 *Preliminary Steps.* Once the DFG SETUP switch is turned on, select the proper settings on the rotary switches at the *rear* of the drawer. The "10 SEG/ 20 SEG/INV" switch should be in the "10 SEG" position, which separates the unit into two independent 10-segment DFG's. The switch marked "MULT" determines the maximum slope change per segment; rules for determining the best setting are covered in Paragraph 10.3.4. For a relatively "mild" function such as the one in Figure 10.2, a setting of "1" is adequate.

10.3.3.6 *Slope Switches.* Turn all slope switches *off* for the DFG being set up.

10.3.3.7 *Setting x and f(x).* Now set up the values of x and f(x), starting from x = 0 and proceeding out from the origin toward the maximum x. The breakpoint value is read directly on the DVM; to read the corresponding function value, depress the appropriate switch. Each switch is momentary; it must be *held* down while setting f(x). When the switch is released, the breakpoint value x is displayed again.

Table 10.2 gives detailed information on which switch to depress at any given time. The table applies to *any* ten-segment function with positive inputs; the values of x and f(x) have been left blank, except for the initial and final values of x, which must be zero and one.

Table 10.2

SEGMENT SELECTOR	X Value	Set X on This Pot	Then Hold Down This Button While Setting Y	Set Y on This Pot and Switch	Y Value
OFF	0.0000	None	PX	PARALLAX	
2		BP2	SLOPE RO	SL1*	
3		BP3	SLOPE RO	SL2	
4		BP4	SLOPE RO	SL3	
5		BP5	SLOPE RO	SL4	
6		BP6	SLOPE RO	SL5	
7		BP7	SLOPE RO	SL6	
8		BP8	SLOPE RO	SL7	
9		BP9	SLOPE RO	SL8	
10		BP10	SLOPE RO	SL9	
OFF	1.0000	None	+ FINAL SLOPE	SL10	

**Use ±CS position, not ±SL position.*

10.3.3.8 *The Pattern of Settings.* Notice that except for the first and last settings, the value of y at any point is determined by the setting on the *previous* slope pot. The reason for this is explained in Paragraph 10.3.2. Note also that BP pot 1 is not set; it is not used in ten-segment operation. This means that position 1 on the SEGMENT SELECTOR is *skipped* (see left-hand column in Table 10.2).

10.3.3.9 *Slope Switch Position.* The table says to "set y on a pot *and* switch." Each slope pot has a slope switch immediately to its left; when setting the function value, the operator first turns on the switch to the +SL or -SL position, and *then* adjusts the pot to obtain the correct f(x) value. If the switch is in the OFF (center) position, the pot has no affect.

How does the operator know whether to use the + or - position? The easiest thing to do is to leave the switch off while depressing the readout button. This displays the function value with the segment turned *off*. This value will not be equal to the desired value at this point. Turning the segment on will increase or decrease this value. If the desired function value is more positive than the value with the segment off, then the switch should be turned to the +SL position. Conversely, if it is desired to *decrease* the function value (make it more negative), then the -SL position should be used. Some people prefer not to memorize this rule, but simply turn the switch on in either direction; if the output moves in the wrong direction, the switch should be reversed. In any case, it is the *direction* of change that is important; the function value should change in the right direction when the switch is turned on. If the switch has no effect on the function value, the slope pot is probably set to zero; give it a few turns and repeat the ON/OFF process.

10.3.3.10 *Trimming Adjustments.* Having set up the entire function, from the origin outward, the operator should now go through the table again, checking the function values f(x). The breakpoints, once set, should remain essentially constant, but the function values may have changed slightly. This is because the value at a given breakpoint is set by changing the slope at the previously set breakpoint, and this causes a small shift in the previously set function value.

The amount of this shift depends upon the nature of the function and the spacing of breakpoints, but it is generally about 0.0010 to 0.0020 unit (10 to 20 millivolts), and rarely greater than 0.0050. In many cases, this shift if negligible. However, if desired, most of this effect may be removed by a series of trimming adjustments. These adjustments should be made in the same order as the original setup - starting at the origin and working outward. The trimming process goes much faster than the original setup, since the breakpoints do not have to be set again, and only small changes in function values are required. After trimming, most function values will be correct to within 0.0002 to 0.0005 unit; rarely is a *second* set of trimming adjustments needed.

10.3.3.11 *Plotting.* Once the function is set, a continuous plot of output versus input should be made, which serves as part of the problem documentation. Such a plot may be made on the 680 without re-patching. The 680 DFG setup panel contains a built-in ramp integrator to provide a smooth sweep for the input. Slide out the upper DFG drawer, and make the appropriate plotter connections at the terminals on the right. Turn on the OFF/ON switch on the left, and set the IC and RATE switches appropriately. To sweep from -Reference upwards, turn the RATE switch to "+". To sweep from +Reference downwards, put the RATE switch to "-"; this reverses both the rate and the IC. To start the sweep at x = 0, turn the IC switch OFF.

To make a plot, put the switch marked RESET/OPERATE to the OPERATE position. The rate of the sweep is determined by the "RATE" pot; a little experimenting will produce a setting that does not overdrive the plotter. When the plot is completed, put the RESET/OPERATE switch to the RESET position and turn the OFF/ON switch OFF.

10.3.4 Insufficient Slope

During the above procedure, it may happen that a particular function value cannot be obtained. If the slope pot is rotated to the end of its travel (ten times) and the function value still hasn't been reached, the first thing to do is to check Table 10.2 and make sure you are setting the right pot. Also, make sure the slope polarity switch is in the right position. Assuming that no such error has been made, the problem is probably one of insufficient slope.

For each segment there is an upper bound to the amount of slope *change* that it can introduce; this is the amount produced with the slope pot fully clockwise. On the 680, a maximum slope change of 1.0 may be obtained with one segment, assuming the slope multiplication switch is in the "1" position (see Paragraph 10.3.3.5). Other positions of this switch allow for slope changes as great as 32.

The slope multiplication switch works by changing the effective feedback resistance on the output amplifier, thus providing greater gain. For very steep or sharply curving functions, a position other than "1" may be necessary. There is also a limitation on the initial slope f' (0). This limitation is 3.0 if the MULT switch is in the "1" position, and it goes up in proportion to the setting on this switch, so that the maximum value is 96 (3×32).

The effective resolution of the slope pots decreases with higher gain; at high settings a small motion of the pot produces a large change in the output, making accurate setup difficult. Also, electrical characteristics such as bandwidth are degraded at high gain settings. For this reason, it is not desirable to use any more gain than necessary in generating a particular function.

A conservative procedure is to set the switch initially at "1", and proceed to set up the function until insufficient slope is encountered, then try a setting of 2 and try again. However, this procedure may lead to a number of false starts, and some method of estimating the maximum slope requirement prior to setup is desirable.

Such an estimate may be easily obtained from a graph of the function once the breakpoint locations have been determined. The procedure is as follows:

1. Locate visually the points where the slope is steepest (in either the positive or negative direction).
2. Estimate the slope of the curve at these points by drawing triangles or counting squares on the graph.
3. Form the difference between the maximum positive slope and the maximum negative slope. This is the total slope change required between the two points where maximum slope occurs. Note that in subtracting two slopes of *opposite* sign, the magnitudes are *added*. If there are several points of maximum positive and negative slope, choose a pair of such points near each other where the difference in slopes is large.
4. Divide the total slope change between these two points by the number of breakpoints in this interval. This gives, with a small amount of effort, the *average* slope change per breakpoint in the "worst case" region. The slope actually required may be somewhat greater, since not all segments will have the same slope change. However, this estimate is a good one to use in practice, as a starting point.

10.3.5 Example of Slope Amplification

As an example of a function requiring slope amplification, see Figure 10.6. This curve was initially drawn free-hand on a sheet of graph paper and inserted in the x-y plotter. Breakpoints and function values were set directly by observing the plotter, not the DVM. Hence there was no need to tabulate the function. Thus the curve offers a good example of graphical setup procedure as well as of slope amplification.

Breakpoint location was determined by following the rules in Paragraph 10.3.1. These are 4 relatively straight portions and 3 relatively "curvy" portions. Since the function appears to curve about the same amount in each curved region, the nine available breakpoints were equally distributed - three per region. Note that the breakpoints have been marked according to the - SEGMENT SELECTOR position that will be used in setting them. The pattern goes: OFF, 2, 3, 4. . . . 9, 10, OFF. As mentioned previously, position 1 is skipped.

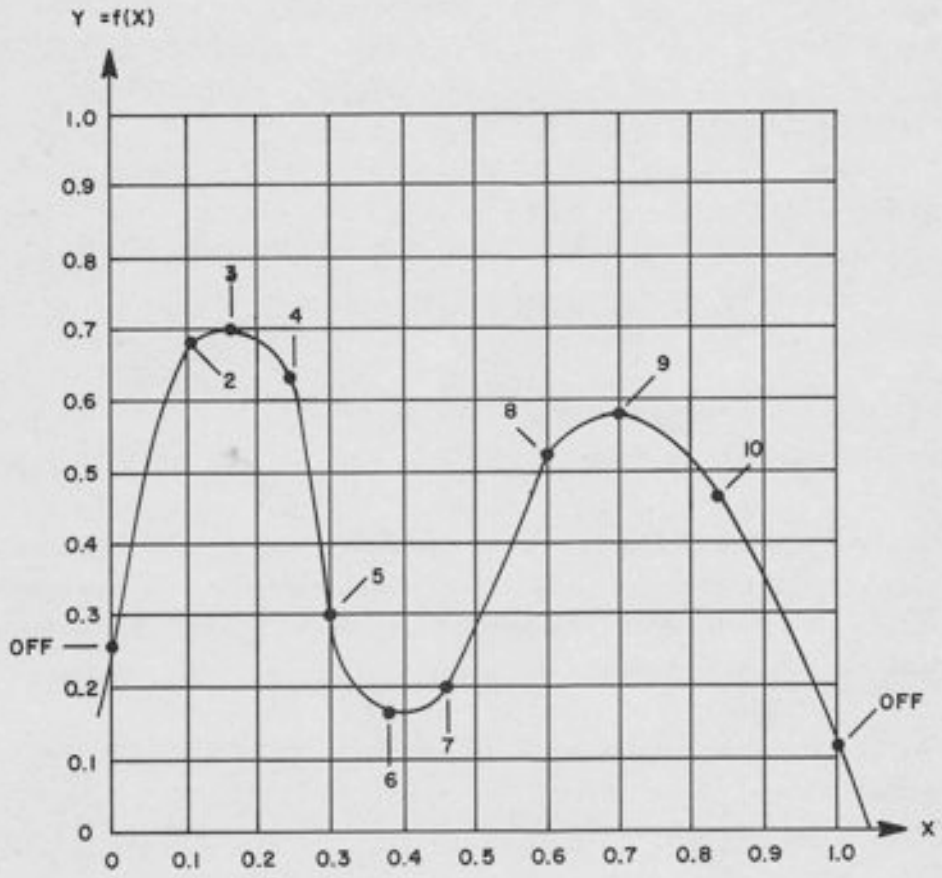


Figure 10.6. Typical Function Requiring Slope Amplification

The greatest positive slope occurs at the left side; the greatest negative slope occurs just past the first peak; these facts are obvious by inspection of the graph.

Graphical determination of the slopes indicates that the positive slope is about 5.5, and the negative slope about -6. The *difference* in slopes is 11.5. Since there are three breakpoints between these two points, the *average* slope change per segment is 11.5/3 or 3.9. It is somewhat questionable whether a slope multiplier of 4 will be adequate, since some of these breakpoints will require greater slope change than others. However, it *may* be possible to get by with 4, especially since the slope rating is somewhat conservatively specified on most DFG's. Hence a setting of 4 was tried.

As might be expected, there was difficulty in setting the value at point 5. The smallest value obtainable was about a quarter-inch above the curve. (About 0.025 unit.) Hence, the slope multiplier switch was set to the next higher value (8) and the setup was repeated. Note that

when the slope amplification is changed, it is necessary to go back to the beginning and re-set *every* previously set function value, starting with the PARALLAX setting, since doubling the gain will double the entire function up to that point. However, the breakpoint settings do not have to be re-set; they are unaffected by the slope amplification switch.

With a slope setting of 8, the setup proceeded smoothly. No difficulty was observed in setting function values. A continuous plot made after the setup was completed indicated that the plotted function was virtually indistinguishable from the original hand-drawn curve over most of its length, and that the maximum deviation was about 0.3%. No trimming adjustments were found to be necessary.

10.3.6 Eleven-Segment Functions

At this point, the reader may be wondering what "Breakpoint 1" is for. The setup procedure calls for ignoring this breakpoint pot and its corresponding position on the segment selector. This breakpoint is usable for twenty-segment functions (see Paragraph 10.3.8) and, under certain conditions, for eleven-segment functions.

Whenever the function to be generated is initially horizontal (that is, $f'(0) = 0$), then the function may be generated with eleven segments instead of ten. The additional segment is horizontal. *An example of such a curve is given in Figure 10.7, and a corresponding table of values is* given in Table 10.3.

Table 10.3

SEGMENT SELECTOR	x	f(x)	SEGMENT SELECTOR	x	f(x)
OFF	0.00	0.33	6	0.46	0.84
1	0.06	0.33	7	0.52	0.84
2	0.12	0.36	8	0.60	0.82
3	0.18	0.42	9	0.70	0.76
4	0.34	0.72	10	0.84	0.60
5	0.40	0.80	OFF	1.00	0.32

Note that since the first segment is horizontal, the value at the first breakpoint is the value at the origin. In fact, since the value at a given breakpoint is set by adjusting the slope at the *previous* breakpoint, there is no control for adjusting the function value at breakpoint number one.

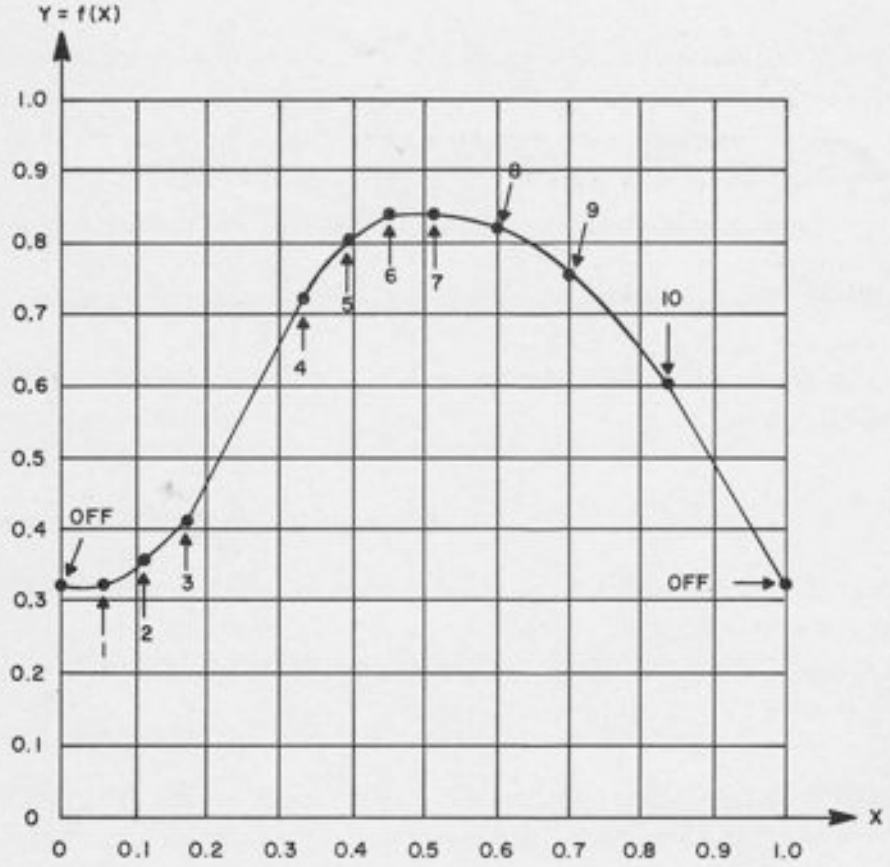


Figure 10.7. Initially Horizontal Eleven-Segment Function

The setup procedure is exactly the same as for any other function, except for the two following exceptions:

1. Position 1 on the SEGMENT SELECTOR is *not* skipped. It is used for setting breakpoint 1. Once the breakpoint has been set, the function value can be read out by depressing the SLOPE RO button, but there is no way to *adjust* this value without disturbing the rest of the function. The value should be equal to the value of x = 0 (previously set by the PARALLAX control), plus or minus a small increment due to interaction with the next setting.

2. The slope switch for BP1 is put in the ±SL position, rather than the ±CS position.

   The reason for this feature is that the slope pot for segment 1 is actually a CENTER SLOPE pot; it is this pot that sets the slope at x = 0. When the pot is used in this manner, there is no diode and hence no breakpoint associated with it. Electrically, this pot simply provides linear gain from

the input to the output. If f' (0) = 0, then there is no need for a pot to set the initial slope. Hence, by adding one more pot, (breakpoint pot 1) an additional segment becomes available. The CENTER SLOPE pot becomes, instead, a slope pot for the extra segment. (Of course, the setting of this pot determines the value of the function at the *next* breakpoint.)

10.3.7 Negative Inputs

The above procedure applies to the +DFG; this type of DFG accepts positive inputs only. The *output* values, however, may be of either polarity. For generating functions with *negative* inputs, the -DFG is used. Most computers are equipped with an equal number of either type; however, they may be installed in any proportions.

The setup procedure for the -DFG is essentially the same as for the + type. One starts from zero, and works *away* from the origin toward the final value of -1.0000. The value at this last endpoint is read by depressing the -FINAL SLOPE button, rather than +FINAL SLOPE. The rule given in Paragraph 10.3.3.9 for determining the polarity of the slope switch should be reversed.

10.3.8 Twenty-Segment Functions

Provision is made for operating a pair of ten-segment DFG's as a single twenty-segment unit. The unused output amplifier of the second DFG is then available for independent use as an inverter. Twenty-segment operation can serve either of two purposes: increased accuracy through the use of more segments, or the generation of functions from an input that ranges over both polarities. For the former purpose, two DFG's of the same type (both "+" or both "-") are used together; for the latter, one "+" and one "-" are used together. In the most common arrangement, the first DFG in a pair is the "+" type and the second is the "-" type. However, either type may be put in any position, so that it is possible to get, for example, twenty breakpoints in the interval $0 \leq x \leq 1$.

The PARALLAX controls on two connected DFG's perform the same function; each of them is simply a bias pot adding a constant (positive or negative) voltage to the output. In twenty-segment operation, only one of these controls is needed, the other one should be turned off.

Similarly, the controls marked CENTER SLOPE (i.e., the ±CS position on slope switch 1) determine the slope at x = 0. This slope is determined by a pot and input resistor; like the PARALLAX controls, one of these is redundant in twenty-segment operation. However, unlike the PARALLAX control, the CENTER SLOPE control may be used as an ordinary segment

when not needed for central slope. This capability has already been described above, in Paragraph 10.3.6, under "Eleven-Segment Functions."

In the case of a DFG with positive and negative inputs, a little thought should be given to the problem of setting the values in the interval around zero. What is desired is a straightforward method of setting the values of x and f(x) at all breakpoints. If there is no breakpoint at x = 0, then the function values of the two breakpoints nearest zero (one positive, one negative) cannot be set directly and independently. Over the interval containing zero, no diodes are conducting, and the output is simply a linear function of the input. The PARALLAX pot allows setting the y-intercept of this function; i.e., the value when x = 0. The CENTRAL SLOPE pot, which is Slope pot 1 on either the + or the -DFG, allows setting the slope of this line. Since these two parameters completely characterize the line, they can be set to pass the line through any two points; i.e., they can be set to give the correct values at the two breakpoints (one positive, one negative).

However, the relation between these two pot-settings shows a good deal of interaction; *each* pot-setting affects *both* values. This interaction does not exist anywhere except in this one interval. Setting any other function value does not disturb previous settings, except for the small secondary effect of the "diode curvature" which is easily taken care of by "trimming" if necessary.

To set the values at the two breakpoints containing zero, first calculate and tabulate f(0), even though this is *not* a breakpoint. The value of f(0) should be calculated by linear interpolation between the values at the breakpoints on either side of zero, since the curve is straight over This interval. Of course, the interpolation can be done graphically simply by drawing a line connecting these points. Once the values have been set at x = 0 and at *one* of the two breakpoints, they should automatically be correct for the other breakpoint.

Since there is no need for two CENTRAL SLOPE pots in twenty-segment operation, one of the two pots can be used for a regular breakpoint. This allows 9 breakpoints to be used on one side of zero, and 10 on the other. The operator may put this tenth breakpoint on either side, depending upon where it is needed most.

As an example, consider the function in Figure 10.8. This function has three regions where it curves rather sharply, separated by regions where it is relatively straight. One of the curved regions lies in the negative half of the graph and another in the positive half. Since the third curved region lies mostly on the positive side, it appears advisable to put the "extra" breakpoint on the +DFG. Hence, BP1 on the -DFG is used for the CENTRAL slope, and BP1 on the +DFG is used as a regular breakpoint. The resulting breakpoint tabulation is given in Table 10.4. Note that the SEGMENT SELECTOR positions for each segment are given on the figure, as well as in the table.

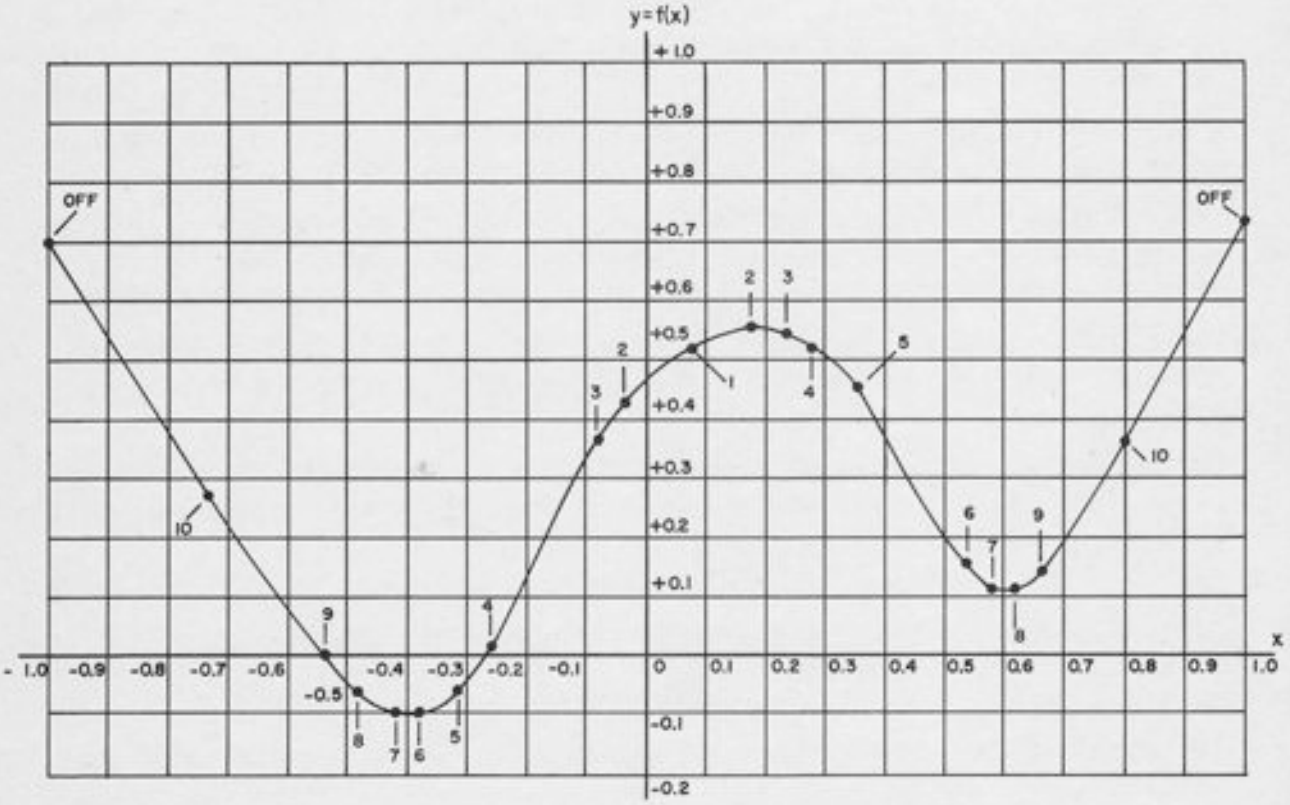


Figure 10.8. A Typical Twenty-Segment Function

Table 10.4

x	f(x)	SEGMENT SELECTOR Position	
-1.00	+0.70	OFF	
-0.74	+0.28	10	
-0.54	0.00	9	
-0.48	-0.06	8	
-0.42	-0.10	7	-DFG
-0.38	-0.10	6	
-0.32	-0.06	5	
-0.26	+0.02	4	
-0.08	+0.38	3	
-0.04	+0.44	2	
0.00	+0.47	OFF	(Both SEGMENT SELECTORS Off)
+0.08	+0.53	1	
+0.18	+0.56	2	
+0.24	+0.55	3	
+0.28	+0.52	4	
+0.36	+0.46	5	+DFG
+0.54	+0.16	6	
+0.58	+0.12	7	
+0.62	+0.12	8	
+0.66	+0.14	9	
+0.80	+0.36	10	
+1.00	+0.74	OFF	

In setting the function, first turn all slope switches off for both DFG's, and put the rotary switch in the back of the drawer to the "20 SEG" position. Address the appropriate output amplifier on the SIGNAL SELECTOR. Since both DFG's are connected to the first amplifier, it is this amplifier (the one whose address ends in -2) that should be addressed. The other output amplifier (the one ending in -7) is disconnected from the DFG, and is available for use as an inverter. Its slope multiplier switch (the one on the right) should be set to 1. A quick calculation based on the technique of Paragraph 10.3.4 indicates that a slope multiplier of unity is probably adequate for this function; hence, the slope multiplier switch on the left should also be set to 1. Set all breakpoints (positive and negative), but do not set function values at this time.

NOTE

Only one SEGMENT SELECTOR should be on at a time. When setting either breakpoints or function values on one of the DFG's, be sure that the SEGMENT SELECTOR on the other one is in the "OFF" position.

Set both SEGMENT SELECTOR switches to the "OFF" position and set f(0). Then put the +DFG SEGMENT SELECTOR in position 1, and set the value at the first positive breakpoint. Turn this SEGMENT SELECTOR off and put the other SEGMENT SELECTOR in position 2 to read the value at the first negative breakpoint. (Note the switch positions, as tabulated in Table 10.4.) When the SLOPE RO button is depressed, the function value at this breakpoint should be correct.

If it is not, then the three tabulated values are not collinear; if this happens, determine the correct f(0) and try again. Once proper values have been obtained at these breakpoints, set the function values on the -DFG, working outward from the origin, and then do the same for the +DFG. Remember to turn off the SEGMENT SELECTOR for one DFG when setting either breakpoints or function values on the other.

Trimming adjustments may or may not be necessary, depending upon the nature of the function and the accuracy required. As with a ten-segment unit, trimming should be done from the origin outward. Remember there is one function value that cannot be trimmed: the PX and CS pots allow the function to be set properly at x = 0 and at *one* of the two breakpoints nearest the origin; the value at the other breakpoint will be close to the desired value, but it cannot be changed without disturbing previous settings.

If it is necessary to trim the function values at the two breakpoints near the origin accurately, an iterative procedure may be used. Trim the function value nearest to zero by means of the PARALLAX pot, trim the other value by means of the CENTRAL SLOPE pot, and alternate

until both function values are correct. The value of f(0) is, of course, no longer equal to the tabulated value, but the values at the two *breakpoints* are correct. The interaction between settings means that after setup, the value of f(0) may no longer be exactly collinear with the adjacent values. Now proceed to trim the other function values, working from the origin outward, as before.

After the last function value is set, be sure both SEGMENT SELECTOR switches are off, and plot the function using the time-base integrator in the VDFG setup drawer. A sweep from -Reference to +Reference should be used to cover the entire range of the function.

If one of the breakpoints occurs at x = 0, then the procedure is somewhat simplified. The zero breakpoint can be set on BP1 for either the + or the -DFG; the BP1 pot on the other DFG is not used, since this segment is used for CENTER SLOPE. The value f(0) is set by a PARALLAX pot as usual; the value at "breakpoint 1" on the DFG being used to give the zero breakpoint should agree with the PARALLAX setting.

10.4 CIRCUIT DETAILS

This section contains circuit information and simplified schematics which will be of interest to some users. However, this information is not required for proper programming, patching, and setup.

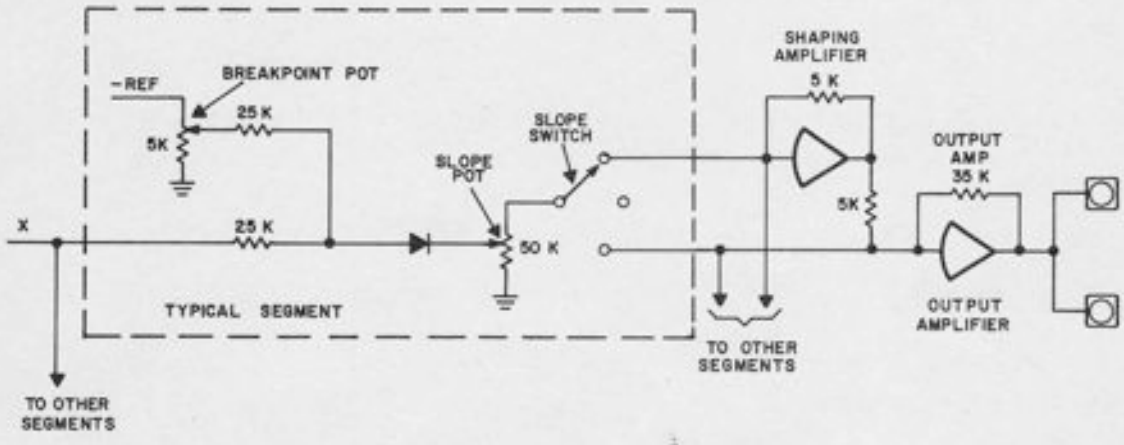


Figure 10.9. Typical Circuitry for One Segment

10.4.1 Circuitry for One Segment

The circuitry for a typical DFG segment is given in Figure 10.9. The circuit is shown for a +DFG; for a -DFG, the diode is reversed and the polarity of the reference bias on the slope pot is also reversed. The analysis below assumes a +DFG.

When the input x is near zero, the negative bias on the breakpoint pot prevents the diode from conducting; the segment therefore contributes nothing to the DFG output. As x becomes more positive, it eventually overrides this bias, and the diode starts to conduct. Thus the bias pot controls the breakpoint.

When the diode is conducting, the output starts to increase or decrease at a rate dependent upon the slope pot setting. The *magnitude* of the slope is determined by this pot; the *sign* of the slope is determined by the SLOPE switch. The overall path from input to output may flow either through one amplifier or two. In the former case, the slope is negative; in the latter, positive. Note that "slope" as used here means "incremental slope." The segments are in parallel, and the actual slope at any given time is the *sum* of all slope contributions (positive and negative).

10.4.2 Circuitry for 10/20/INV Selection

At the rear of the DFG drawer is a switch for each DFG pair marked "10/20/INV." This switch selects one of the three modes of operation: either 2 ten-segment DFG's, 1 twenty-segment DFG and 1 inverter, or 2 inverters. Figure 10.10 shows the appropriate internal circuitry. Each DFG contains ten segments and one output amplifier. (The "shaping amplifier" shown in Figure 10.9 is not shown in Figure 10.10. Each box marked "10 SEGMENTS" in Figure 10.10 contains a shaping amplifier.)

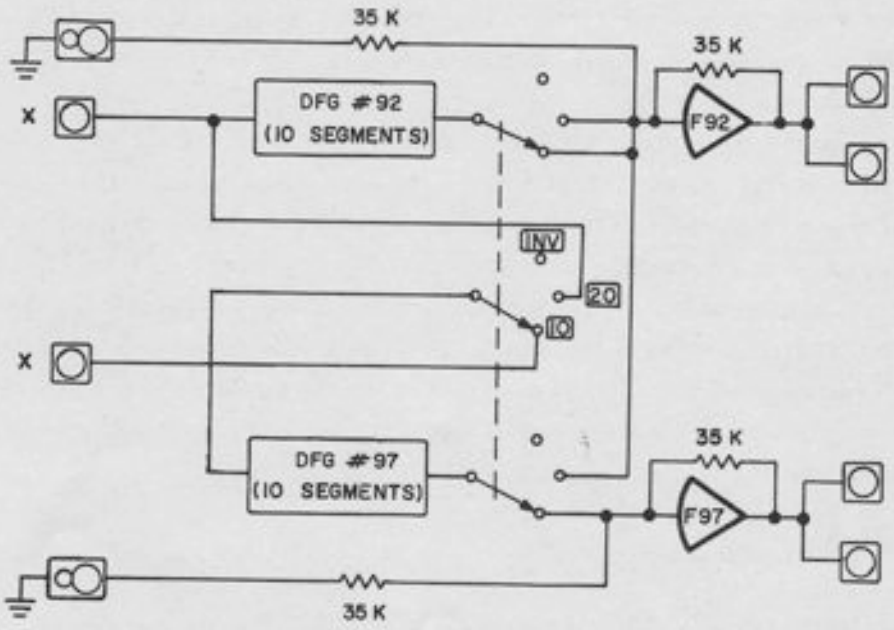


Figure 10.10. 10/20/INV Switching

In the *10 seg* mode, each DFG is connected to its own amplifier and to its own inputs. The units function completely independently. Each DFG has an additional input resistor terminated on the patch panel, which allows the addition of another variable to the DFG output without the use of an additional summer.

In the *20 seg* mode, the segments for DFG 97 are connected to the patch panel input and the output amplifier for DFG 92. Hence, F92 becomes a 20-segment DFG, and amplifier F97 has no segments connected to it. The input resistor terminated on the patch panel allows an amplifier F97 to be used as a gain-one inverter.

In the *inv* mode, all DFG segments are disconnected from their output amplifiers; both amplifiers (F92 and F97) may be used as inverters.

10.4.3 Slope Multiplication Circuitry

In previous schematics (Figures 10.9 and 10.10) the feedback resistor for the DFG output amplifier is shown as a fixed resistor. However, there is a slope multiplication switch for each 10-segment DFG which changes the effective feedback resistance, increasing the slope change obtainable for a given segment. This switch has six positions, labeled in ascending powers of 2: 1, 2, 4, 8, 16, and 32. In the "1" position, the standard feedback resistance is connected (35K). Each segment can produce a slope change of up to ±1.0. In the other positions, the feedback network is modified to permit greater slope changes, up to a maximum of 32. Paragraph 10.3.4 contains information and an illustration on the use of this switch.

The use of the extra input resistor for combined summation and function generation is not recommended as a general practice if the function to be generated requires a slope amplification factor greater than one. Although it *can* be done, the effective gain for this input is multiplied by the setting on the slope multiplication pot; in the "8" position, for example, the input provides a gain of approximately 8. Furthermore, only *the "1" position* provides a feedback resistor matched against the input resistor to 0.01%; in all other positions, the tolerance on the feedback resistance is 5%. This is of no consequence in function generation, since the DFG is set up by observing the actual amplifier output, and hence, feedback resistor tolerance is not crucial.

10.4.4 Setup Panel Circuitry

The setup panel, whose operation is described in Paragraph 10.3, allows direct DFG setup in terms of breakpoint values and function values. Readout of f(x) is accomplished by direct monitoring of the DFG output amplifier on the signal selector; however, some additional external

circuitry is required to set up *breakpoints*. Figure 10.11 shows a simplified schematic of the circuitry. The key to the circuit lies in the fact that the breakpoint of any given segment is the value of the input at which the diode just begins to conduct; this means that the junction point of the input and bias resistors for that segment is at zero potential. (This analysis assumes an "ideal" diode. Actually, each segment contains circuitry to provide compensation for the non-ideal diode characteristic. For simplicity, this circuitry is omitted from Figure 10.11.)

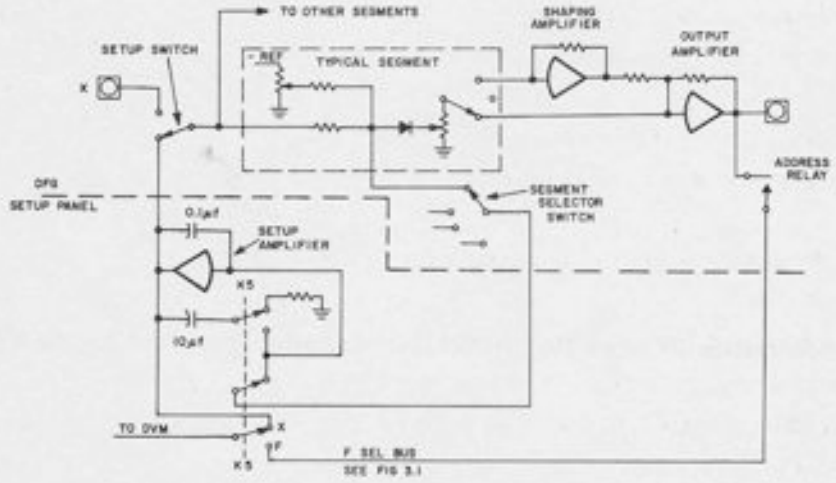


Figure 10.11. Setup Panel Circuitry

When a DFG breakpoint is being set, the SEGMENT SELECTOR switch connects this junction point to the summing junction of a high-gain amplifier in the DFG setup panel. The amplifier output is also connected to the DFG input, so that the DFG segment is in the feedback loop of the amplifier. The input resistor is now acting as a feedback resistor for the amplifier, and the BREAKPOINT pot and bias resistor provide an input. As the BREAKPOINT pot is adjusted, the amplifier output changes in response. Hence, the output of the setup amplifier is always equal to the value which makes the summing point zero; i.e., it is always equal to the breakpoint value.

The relay marked K5 is controlled by the SLOPE READOUT button. When it is depressed, the breakpoint value is stored on a 10μf capacitor, so that the setup amplifier is in the *hold* mode while the relay is energized.

Note also that when the K5 relay is energized, the connection between the junction point and the setup amplifier is broken, and the DFG reverts to normal operation. Its input is the breakpoint value, and its output is the corresponding function value at that point. Note from the lower set of contacts on K5 that when it is energized, the DVM reads the selected DFG, rather than the setup amplifier. Hence, the effect of K5 is to allow direct readout of either the breakpoint x or the output f(x).

CHAPTER 11

THE MULTIPLIER

The 680 has provision for 24 multipliers. All are the quarter-square type, and have output amplifiers associated with them. The output amplifier and the multiplier may be disconnected and used independently, if desired. Each multiplier may be separated into two independent squaring or square-root circuits.

11.1 LOCATION AND ADDRESSING

All trays whose address ends in -3 or -8 are multiplier trays. This gives a total of 24 such trays in a fully expanded computer.

11.2 APPLICATIONS

The 680 multiplier may be used for multiplication, division, and generating squares and square roots. Certain other applications, such as generating $x \cdot |x|$, are also possible; see A1.10 and A1.12 for symbols and patching.

11.3 CIRCUIT DETAILS

A quarter-square multiplier works by means of the identity:

$$xy = \left(\frac{x+y}{2}\right)^2 - \left(\frac{x-y}{2}\right)^2$$

Thus a quarter-square multiplier contains two squaring networks: one to generate $\left(\frac{x+y}{2}\right)^2$ and the other to generate $\left(\frac{x-y}{2}\right)^2$.

Normal use of the unit (for multiplication) requires that *each* DFG receive inputs from both x and y, since the first must generate an output proportional to $\left(\frac{x+y}{2}\right)^2$ and the second must generate an output proportional to $\left(\frac{x-y}{2}\right)^2$.

Using the multiplier for generating squares or square roots requires a reconnection of the inputs; one DFG receives only $\pm x$ inputs, and the other receives only $\pm y$ inputs.

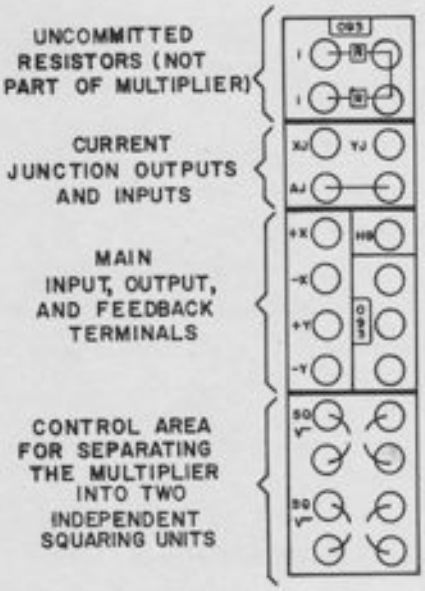
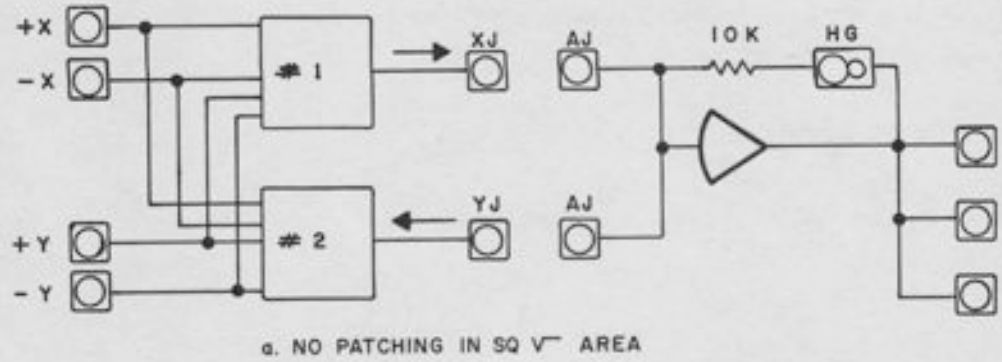
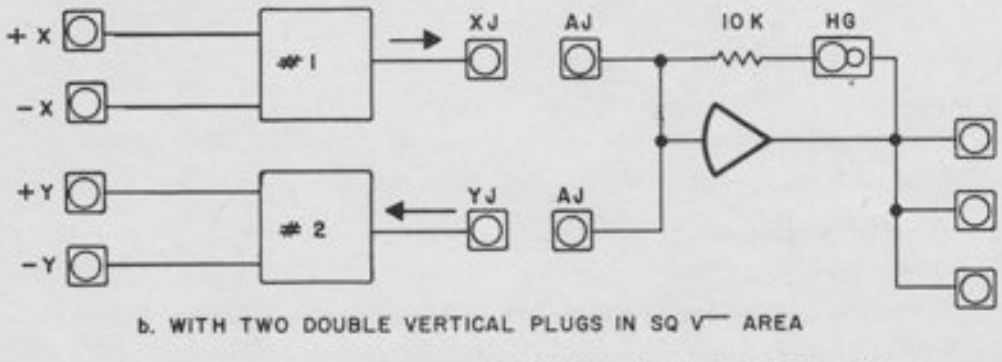


Figure 11.1. Quarter-Square Multiplier Patching Area

On the 680, this switching is performed by normally-closed patch panel connectors terminating in eight terminals at the bottom of the multiplier tray (see Figure 11.1). If nothing is patched into these terminals, the inputs ±x and ±y are connected to both DFG's giving the equivalent schematic in Figure 11.2a. If two double-vertical plugs are inserted in these terminals, the internal connections are re-arranged to give the equivalent schematic of Figure 11.2b. Note that in Figure 11.2b, DFG 1 receives only ±x inputs and DFG 2 receives only ±y inputs.



a. NO PATCHING IN SQ $\sqrt{\ }$ AREA



b. WITH TWO DOUBLE VERTICAL PLUGS IN SQ $\sqrt{\ }$ AREA

Figure 11.2. Quarter-Square Multiplier Equivalent Schematics

In multiplication (or division), with no patching in the eight control terminals, DFG 1 produces an output current proportional to $\left(\frac{x+y}{2}\right)^2$ and DFG 2 produces an output current proportional to $\left(\frac{x-y}{2}\right)^2$. The output junctions, XJ and YJ, are patched to the output amplifier junction, and the output amplifier produces an output voltage proportional to the sum of these currents, i.e., proportional to the product xy. When used with an amplifier with 10K feedback (such as the associated output amplifier) the unit produces the output -xy, where x and y are measured in units (reference voltage = 1.0000 unit). If inputs and outputs are measured in *volts*, then the output is -xy/10. In any case, the scaling is such that if x and y are simultaneously at their maximum values (±reference voltage), then the product is also at its maximum value, (±reference voltage).

Note that the output amplifier is arranged for bottle-plug connection to the multiplier; a double-vertical plug connects both XJ and YJ to the output amplifier. Since the most common uses of the multiplier are for multiplication and division, it is recommended that this plug be left in place when the problem is unpatched. It need only be removed for square or square root generation, or for other special applications. Hence in most cases, no "setup" patching will be required -- only the patching of the inputs ±x and ±y.

For some applications, it is desirable to use the multiplier with some amplifier other than the associated output amplifier. For example, in trigonometric resolution, two or more multipliers are connected to the AJ of one amplifier. In such cases, both XJ and YJ should be patched to the AJ of the other amplifier; the associated amplifier is completely free and may be used for other applications.

The output amplifier has a 10K feedback resistor, which is connected to the amplifier output through normally-closed patch panel contacts. Inserting a pin into the terminal marked "HG" removes this feedback, making the amplifier a *high-gain* amplifier. If an input voltage (instead of a pin) is patched in, the feedback resistor becomes an input resistor; this fact is useful for division and square roots. The output amplifier schematic is very similar to the schematic for the junction inverter covered in Paragraph 9.1; in fact the only difference is the absence of an input resistor.

When the output amplifier is not being used with the multiplier, it may be used as a high-gain amplifier by inserting a pin into the "HG" terminal, or it may be used as the output amplifier for a log/exponential DFG, since it has the necessary 10K feedback. By patching additional resistors to the AJ, it can be used as an inverter or summer, although this should rarely be necessary, since regular summers and combination amplifiers are available.

When eight terminals at the bottom of the tray are covered with two double-vertical bottle plugs, DFG 1 receives ±x inputs, and DFG 2 receives ±y inputs. DFG 1 produces an output current proportional to x^2, and DFG 2 produces an output current proportional to y^2. If each of these DFG's is patched to an output amplifier with 10K feedback, the amplifier outputs will be $-x^2$ and $+y^2$, both on a unit scaled basis. The two DFG's are completely independent. Under some conditions, it is not necessary to provide both signs of the input. DFG 1 responds to positive inputs; if x is always ≥ 0, it is not necessary to furnish -x; simply ground the -x input and patch only the +x input. Similarly, DFG 2 responds to negative inputs; if y is always ≤ 0, ground -y and patch only the +y input. Patching diagrams and symbols are given in Appendix 1.

CHAPTER 12

MISCELLANEOUS ANALOG COMPONENTS

12.1 THE FEEDBACK LIMITER

12.1.1 Location and Addressing

The 680 has provision for 12 feedback limiters. Every tray whose address ends in -1 may contain a feedback limiter. A limiter bears the address of the tray in which it is located. Hence the limiter addresses are 1, 11, 21, 31, 41, 51, 61, 71, 81, 91, 101, and 111. Every feedback limiter is arranged for easy bottle-plug patching to the summer in the same tray (Figure 12.1); however, the limiter may be used to limit the output of *any* amplifier whose amplifier junction appears on the patch panel.

12.1.2 Patching

The feedback limiter is a two-terminal device; its terminals are labeled LJ (Limiter Junction) and FB (Feedback). The FB terminal is patched to the output of the amplifier to be limited, and the LJ is patched to the appropriate junction. For a summer, the appropriate junction is the AJ (Amplifier Junction), or the RJ (Resistor Junction). Since the standard connection for a summer is to patch the amplifier junction to the junction of the associated resistor network, the two terminals are equivalent in normal summer operation. Note that each summer has its RJ terminated twice; once in the control area at the top of the tray, where it is normally covered by a bottle-plug, and once immediately below the control area. Hence an additional connection (such as a feedback limiter) may be made without disturbing the bottle-plug connection.

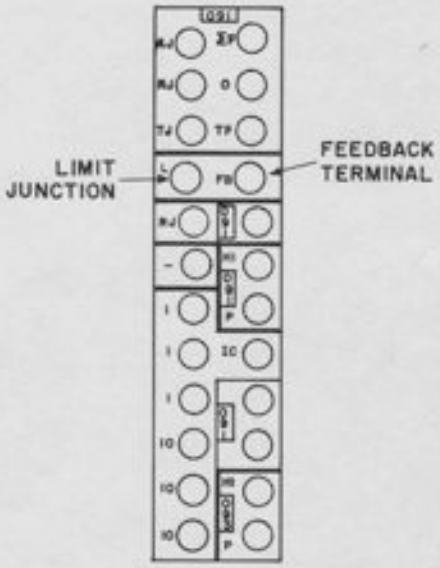


Figure 12.1. Patching Terminations for a Feedback Limiter

For a track/store unit, the appropriate junction is the TJ (Track Junction). Since this is usually bottle-plugged to the RJ, the RJ may be used for the Limit Junction connection, just as with a summer.

To limit the output of an integrator, the OJ (Operate Junction) should be used. This is usually connected to the ∫J (see Paragraph 6.5). Since neither the ∫J nor the OJ is duplicated on the patch panel, a multiple connector will usually be required to connect additional inputs or the LJ of a feedback limiter.

If it is desired to limit the IC of an integrator (a rare occurrence) the LJ should, of course, be used.

12.1.3 Setup Procedure

The two limit points (positive and negative) may be set independently. The limits are controlled by two potentiometers for each limiter. These potentiometers are in the uppermost slide-out drawer to the right of the operator, immediately above the DFG's.

To set a limiter, put the computer in the *PC* mode and open the drawer (Figure 12.2). To set the -limit, depress the button marked - adjacent to the limiter knob, and adjust the knob until the appropriate limit value appears on the DVM. Then release the button and adjust the "+" limit similarly. For example, if the limits are set to -0.3000 and +0.5000, then the output of whatever amplifier the limiter is patched to will be limited between -0.3 unit (-3 volts) and +0.5 unit (+5 volts). It is not necessary to have the limiter actually patched to the amplifier during setup; in fact, the limiters may be set up with the patch panel off.

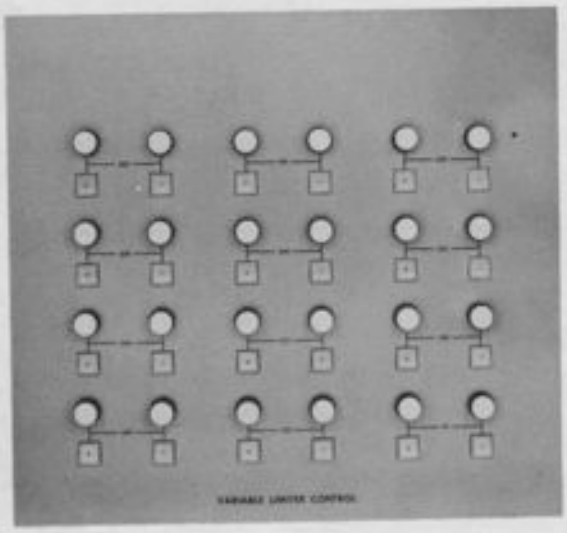


Figure 12.2. Feedback Limiter Setup Controls in Slideout Drawer

12.1.4 Circuit Details

The 680 feedback limiter contains an active network in addition to resistors and diodes. The use of an active network to provide gain in the feedback path makes the limit much "flatter" than it would be with purely passive circuitry. This network is located in the limiter tray immediately behind the patch panel, thus avoiding the necessity of trunking the LJ to the patch panel through many feet of cable, with consequent deterioration of dynamic performance and stability. The only re-

motely located components are the pots in the slide-out drawer. These pots provide positive and negative bias inputs to the limiter in the tray to determine the limit points.

12.2 THE NOISE GENERATOR

The 680 patch panel provides terminations for a dual-channel Gaussian noise generator for statistical studies. The low-frequency output is useful for low-speed runs; the high-frequency output is for high-speed repetitive and iterative operation. The noise generator outputs are terminated in two terminals marked "L" and "H" (for Low and High frequency) in the strip area immediately above tray 70. Further information on the specifications of the noise generator is not available at this time.

12.3 UNCOMMITTED RESISTORS AND DIODES

Uncommitted resistors are available for general-purpose use (for use as additional inputs to summers and integrators, for the construction of special networks, or for any other application). They appear in pairs; the two resistors in a pair are connected to a common junction. A pair of "Gain 1" resistors (100K) appears at the top of each multiplier tray; thus there are 24 such pairs, or 48 "Gain 1" resistors in a fully expanded computer. A pair of "Gain 10" resistors (10K) appears at the top of each DFG tray; thus there are 18 such pairs, or 36 "Gain 10" resistors in a fully expanded computer.

In addition a "Gain 100" resistor (1K) appears in each log/exponential DFG tray. This resistor is *not* one of a pair. These resistors are useful for such applications as generating wide-range exponentials (see Appendix 5); this explains their location in the log/exponential DFG tray. The resistors may also be used as input resistors for summers and integrators, if very high gains are required. However, such use is rare; usually the requirement for a gain of 100 is an indication of poor scaling. (Note that high gains on summers may also be obtained with pot feedback, and high gains on integrators may be obtained by selecting a smaller-than-normal integrating capacitor.)

Since a 1K resistor draws 10 ma of current from a ten-volt source, some care should be taken that the amplifier driving the "Gain 100" input is not otherwise heavily loaded. (Amplifiers on the 680 have an output capability of about 30-35 ma, sufficient to drive almost any load encountered in a practical problem.) Excessive amplifier loading will cause deterioration in performance, but will not permanently damage the amplifier.

A pair of uncommitted diodes is terminated in each sin/cos DFG tray. These diodes may be used for limiting, switching, etc., as desired by the programmer. Note that most limiting and switching functions can be performed better by the feedback limiters, the hard-zero limiters built into the summers and JI's or by the logic elements and electronic switches in the interface tray. There is comparatively little need for a large number of uncommitted diodes, but a few are included for use in special circuits.

12.4 TRUNKS

The 680 Console is provided with 120 trunk lines, numbered T0 through T119. The trunk lines terminate in connectors in the rear of the machine; they may be used to trunk signals between computers, or to connect any desired external devices to the computer. Note that recorders, plotters, the noise generator and conversion equipment for hybrid computation all have their own assigned terminals on the patch panel; it is not necessary to use general purpose trunks for these components.

The trunks are bi-directional, that is, they may be used to provide inputs from an external source or outputs to an external load. The signal on any trunk may be read on the DVM by addressing the trunk on the signal selector; e.g., T37 or T114.

The trunk terminals are located in the strip area between the rows of trays. They are arranged in blocks of ten-ten trunk lines terminating either below of above a given field. Trunks 0, 10, and 20 are *below* the correspondingly numbered trays; trunks 30, 40, and 50 are above. Trunks 60, 70, and 80 are below, and 90, 100 and 110 are above the correspondingly numbered trays. Since each of the trunks ending in -0 begins a block of ten, trunks such as 37 or 104 may be easily located by first locating trunks 30 and 100 and then counting to the right. Every trunk terminal is labeled with its appropriate address.

12.5 REFERENCE, TEST REFERENCE, AND GROUND

The principal output terminations for reference are in the tray areas adjacent to the pots. Every combination amplifier tray has a +Reference terminal and every summer tray has a -Reference terminal. These terminals are arranged to allow easy bottle-plug connections to the nearby pots; this feature makes IC patching for integrators and track/store units especially easy. Every interface tray contains both + and -¡Reference terminations, arranged for easy connection by a bottle plug or short patchcord to the comparator or the nearby pot. Of course, the reference terminals need not be patched to the nearby pots; they may be used anywhere in the problem where ±Reference voltage is required. In addition to the terminations in the trays there are reference terminals in the strip areas below trays 8, 18, 28, 68, 78, and 88.

Test reference output terminations appear in the strip area below trays 34 and 35, 45 and 46, and 55 and 56. The test reference terminals provide ±Reference voltage *only* in the static test mode; this feature is useful in static tests, for providing test outputs for integrators whose regular problem IC's are zero.

Ground terminals appear in the center strip beneath trays 36, 47, and 57; there are four ground terminations under each of these trays. Note that many applications that would require ground terminations on other computers do not require them on the 680. Probably the most common use of ground terminations in most computers is to ground a three-terminal pot to allow its use as a conventional attenuator; this need is eliminated on the 680 by use of normally-closed contacts, as described in Paragraph 8.1.2.

12.6 READOUT DEVICES

12.6.1 Plotters

Terminations are provided for four x-y plotters on the 680 patch panel. Analog inputs for these plotters are found in the strip area under tray 37 (two plotters) and under trays 48 and 57 (one plotter each). Logic control terminals for these plotters are found in the digital strip area underneath the interface control tray in logic field 5. Each terminal controls the pen-lift of one of the x-y plotters - a logic ONE puts the pen down; a logic ZERO raises it. When not patched, these terminals are normally high.

12.6.2 Recorders

Terminals are provided on the patch panel for two eight-channel strip-chart recorders (oscillographs). Each of these recorders can plot eight analog signals and two logic signals versus time. The analog inputs for the first recorder are in the strip area below trays 38 and 39. The analog inputs for the second are in the strip area below trays 58 and 59.

Logic inputs for the recorders are located in the digital strip below the AND GATE tray and the COUNTER tray in logic field 5. Terminals marked "EVTL" and "EVTR" are the logic inputs which are recorded on the "EVENT MARKERS" at the left and the right of the recorder paper. A terminal is also provided for turning the recorder ON under logical control, and four terminals for changing the speed of the paper.

12.6.3 Scopes

Terminals are provided for two oscilloscopes. The analog scope (called DISPLAY SCOPE) accepts up to 18 analog signals and displays any 4 of them simultaneously. The 18 inputs are numbered 0-17 and appear in the strip area beneath trays 9, 19, 29, 69, 79, and 99. Two horizontal inputs (for cross plotting) are also provided; they appear in the strip area along with the other analog inputs. They are labeled H0 (X3) and H3 (X4). A trigger (sync) input for the display scope appears in the logic strip beneath the GPR tray in logic field 5.

The digital (or monitor) scope displays up to four logic signals at a time; it can also be used to display analog signals. Its inputs are terminated in the logic strip area beneath the interface control tray in logic field 2 and the integrator control tray in field 3. Additional inputs are located beneath the GPR and GATE trays in field 5. Two horizontal inputs to the monitor scope are provided, designated H4 and H5. These terminals appear beneath interface trays 79 and 99.

CHAPTER 13

THE INTERFACE TRAY

The interface tray contains the basic components that allow intercommunications between analog and logic signals, namely, comparators, relays, and electronic switches. In addition, each interface tray contains a Junction Inverter (described in Paragraph 9.1) and terminations for a pot (described in Paragraph 8.1). Only the actual interface components will be described here.

13.1 LOCATION AND ADDRESSING

Each tray ending in -4 or -9 is an interface tray (Figure 13.1). Thus there are 24 interface trays in the entire computer.

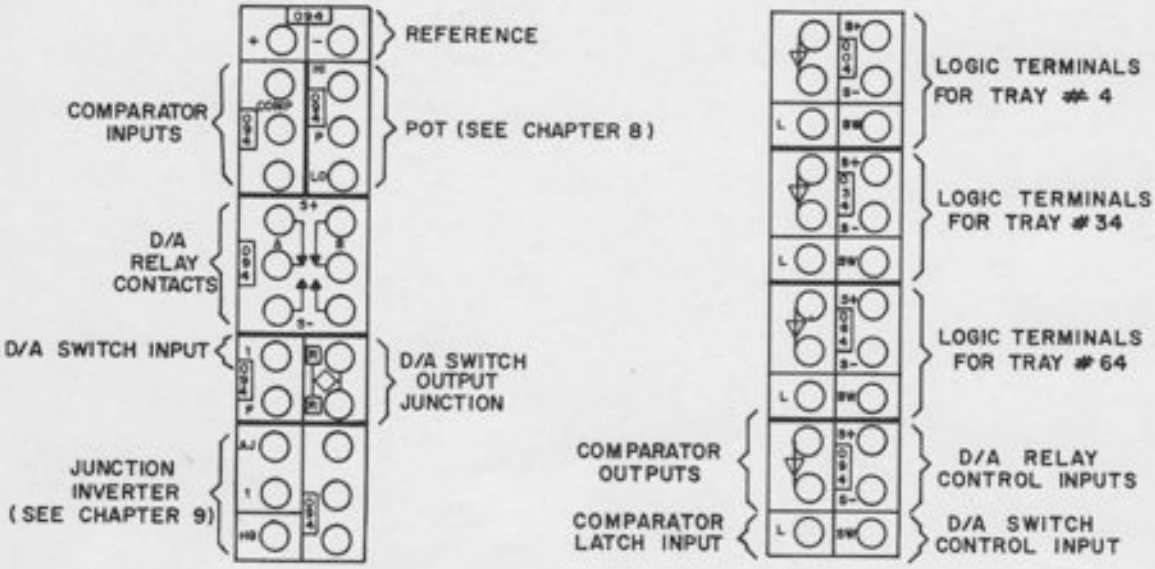


Figure 13.1. Interface Tray Terminations

13.2 THE ANALOG-TO-DIGITAL COMPARATOR

13.2.1 Function

Each interface tray contains an electronic comparator, which accepts analog inputs and produces a logic output. The logic output is high (logic ONE) whenever the sum of the analog inputs is positive, and low (logic ZERO) when the sum of the analog inputs is negative. Three analog inputs are provided for each comparator. It is *not* necessary to ground unused analog inputs. For example, if it is required to compare a single voltage to zero (to determine whether the voltage is positive or negative), it is not necessary to ground the unused terminals. Note, however, the exception to this rule given in Paragraph 13.2.3.

The output appears in the logic patching area. It is synchronized with the system clock. The inverted output is also provided. A latch input appears in the logic area immediately beneath the outputs. If this terminal is high (logic ONE) the comparator output is *latched;* that is; it will not change regardless of the analog inputs. When this terminal is low (logic ZERO) the output follows the analog inputs in the usual manner. If the LATCH input is not patched, it is normally low.

Since the comparator outputs are synchronized with the system clock, they remain constant when the computer is in the *stop* mode.

13.2.2 Readout and Manual Control

The analog readout panel contains pushbutton/indicators which allow visual readout of the state of any comparator, and also allow manual forcing of the comparator output into either state. These controls are described in Paragraph 2.5.2. Note that the manual controls override the analog inputs, the LATCH input, and the digital mode; the comparator may be manually forced into either state in any mode.

13.2.3 Circuit Details

Figure 13.2 is a block diagram of the internal circuitry in the electronic comparator; it is not intended to be an accurate schematic, but it explains the major components. The three analog inputs pass through input resistors to the junction of a high-gain amplifier. This amplifier is not a regular operational amplifier, and is not included in the total amplifier count of 156; if it were, the 680 would be considered a 180-amplifier machine. The amplifier output is always at one of its extreme values, depending on the net analog input. Since the net analog input can

change at any time, the output of this amplifier can switch from one extreme to the other at any time, even between clock pulses. The amplifier output is followed by a clocked flip-flop, so that the logic output on the patch panel is properly synchronized. The LATCH input inhibits this flip-flop from changing state.

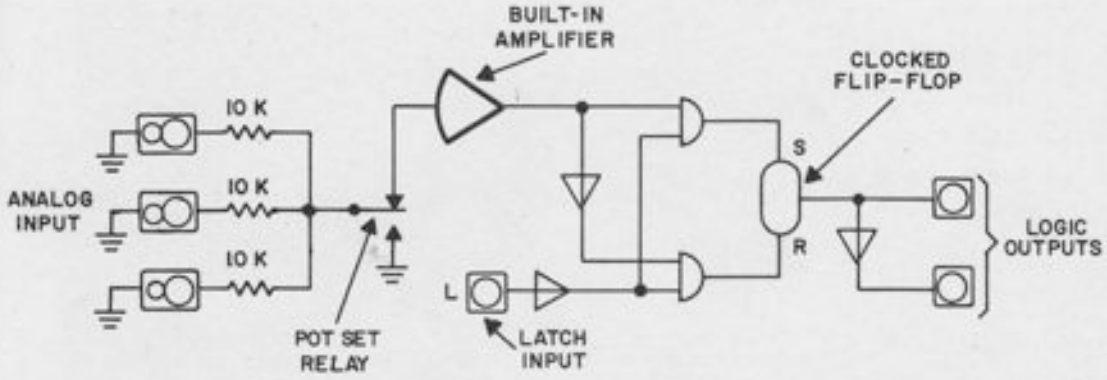


Figure 13.2. Block Diagram, Electronic Comparator

13.2.3.1 *Unused Inputs.* Like most comparators, the 680 comparator performs best (with respect to response time, noise sensitivity, and offset) if its unused inputs are grounded. However, the programmer need not worry about this, in most cases, since the unused inputs are grounded through normally-closed patch panel contacts. The only time this consideration becomes important is when a set of relay contacts is used at a comparator input; in this case, the programmer should arrange the circuit so that if an input is "switched out," it is grounded, rather than left floating.

13.2.3.2 *Loading Errors.* Since the comparator amplifier is not a regular operational amplifier, its summing junction is not always at virtual ground potential. This can cause loading errors if pots are used as comparator inputs. When the comparator is functioning normally, the summing junction will be slightly positive when the net comparator input is positive, and slightly negative when the net comparator input is negative. When the net comparator input is zero, that is, *at the moment of switching,* the summing junction is at zero potential, and the loading on the input pots is correct. Hence, the comparator switches at the correct point, because the loading error is zero at the switching point. A pot-set relay is provided to assure that the pot is always set under the proper load. Hence, for most applications, the programmer need not concern himself with loading problems. However, if a pot feeds *both* a comparator *and* some other amplifier, its output will be slightly in error when the comparator is not at the switching point. In such cases (fairly rare) an additional amplifier should be used to drive the comparator.

Note also that, because of the pot-set relay, the comparator output will not be correct in the *SP* and *PC* modes.

13.3 THE DIGITAL-TO-ANALOG SWITCH

The D/A switch is an electronic switch for high-speed switching of problem variables. It may be thought of as a switchable input resistor; that is, it should be used as an input resistor to an amplifier.

The analog input voltage is patched into the terminal marked "1". This output may come either from an amplifier or from a pot; the input resistance at this terminal is a constant 10K load to ground.

The output terminal on the right should be patched to an amplifier, and serves as an input resistor for this amplifier. The connection should be made to the appropriate junction (AJ, OJ, TJ, or IJ) depending upon the type of amplifier; in any case, it should be patched to the same junction as a regular input resistor. The terminal marked "F" is not used in normal operation.

The logic control input is in the logic patching area. When it is high (logic ONE) the switch is conducting, and when it is low (logic ZERO) the switch is off, and the input makes no contribution to the output. However, even when the switch is off, the input load is still 10K; this is accomplished internally by a second electronic switch which shorts the 10K resistor to ground when it is not connected to the amplifier.

Note that the resistor is a "gain 10" (10K) resistor. It will produce a gain of 10 when used with a summer or integrator, and a gain of 1 when used with a Junction Inverter, since the Junction Inverters use 10K feedback.

A relay equivalent for the D/A switch is shown in Figure 13.3. The actual switching is, of course, electronic.

13.4 THE DIGITAL-TO-ANALOG RELAY

The D/A relay (or function relay) is a relay which can be positioned either manually or by logic signals. It is a DPDT relay, whose contacts terminate in the analog area. It is driven by a flip-flop, which may be set or reset by logic inputs patched into the terminals marked "S+" and "S-" in the logic area. If the "S+" input is high (logic ONE) the relay is set to the + state; if the

S- input is high, it is set to the "-" state. If both S+ and S- inputs are low (logic ZERO), the relay remains in the state to which it was last set. The programmer should arrange his program so that the S+ and S- inputs are not both simultaneously high.

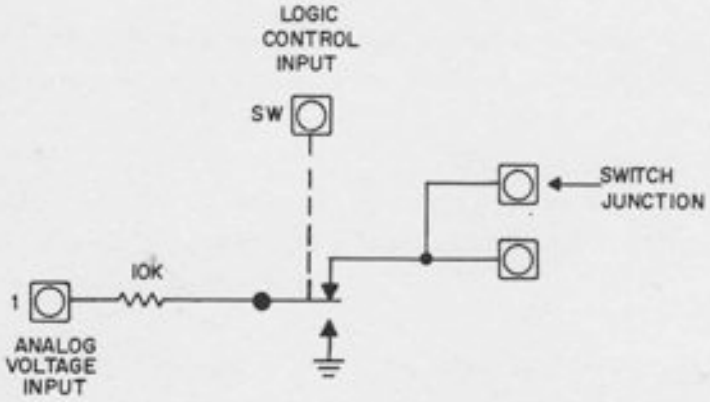


Figure 13.3. Relay Equivalent of D/A Electronic Switch

For most applications, the S+ and S- inputs are complementary; that is, some logic signal is patched into S+ and the inverted signal is patched into S-. Under these conditions the relay follows the S+ input. The relay contacts are labeled "+" and "-" to correspond to the logic inputs S+ and S-. The notation S+ and S- was chosen with the electronic comparator in mind; if the normal and inverted outputs of a comparator are patched to the S+ and S- inputs respectively, the relay will be in the "+" position when the net comparator input is positive and the "-" position when the net comparator input is negative.

The function relays have indicators on the analog readout panel which indicate the state of each relay; the indicator is lit when the relay is in the "+" position. These indicators also provide a means for manual control - a relay may be forced to either the "+" or "-" position by pushing the appropriate button. This feature enables the relays to be used as manually-positioned function switches if nothing is patched into the logic input terminals; see Paragraph 2.5.2 for details of manual control.

MANUAL REVISION NOTICE*

ELECTRONIC ASSOCIATES INC.
LONG BRANCH NEW JERSEY

PAGE	ITEM / PARA	REVISION
13-5/ 13-6	11.6	At bottom of page, add the following: CAUTION When switching reference through a function relay, it should always be patched through a buffer stage to prevent possible damage to relay contacts.

DATE 2/23/71	MANUAL TITLE 680 Reference Manual Publ. No. 00.800.2048-3	REVISION NOTICE NO. SH. 1 OF 1 SH.

* THIS MANUAL REVISION NOTICE IS ISSUED TO INCORPORATE IMPROVEMENTS OR CHANGES OF ROUTINE OR MINOR NATURE IN THE SUBJECT MANUAL.

CHAPTER 14

THE GATE TRAY

14.1 LOCATION AND ADDRESSING

The 680 logic section has provision for a total of 36 general-purpose AND gates; 6 per field. The gates in a given field are labeled A-F. Gate A is located at the bottom of the integrator control tray at the left of the field, and gates B-F are located in the GATE tray in the middle of the field (Figure 14.1). Gate F is a six-input gate; the other five are two-input gates. Unused inputs need not be patched. The address of a gate consists of a digit (0-5) indicating the field, and a letter (A-F) specifying the gate within the field. Hence, typical gate addresses are 0A, 1A, 2F, etc.

Every gate has an indicator light on the logic readout panel, which lights when the gate output is high (logic ONE). The gate indicators are described in Paragraph 2.3.4.

14.2 APPLICATIONS

In addition to the AND function, the gates may be used for a number of other purposes.

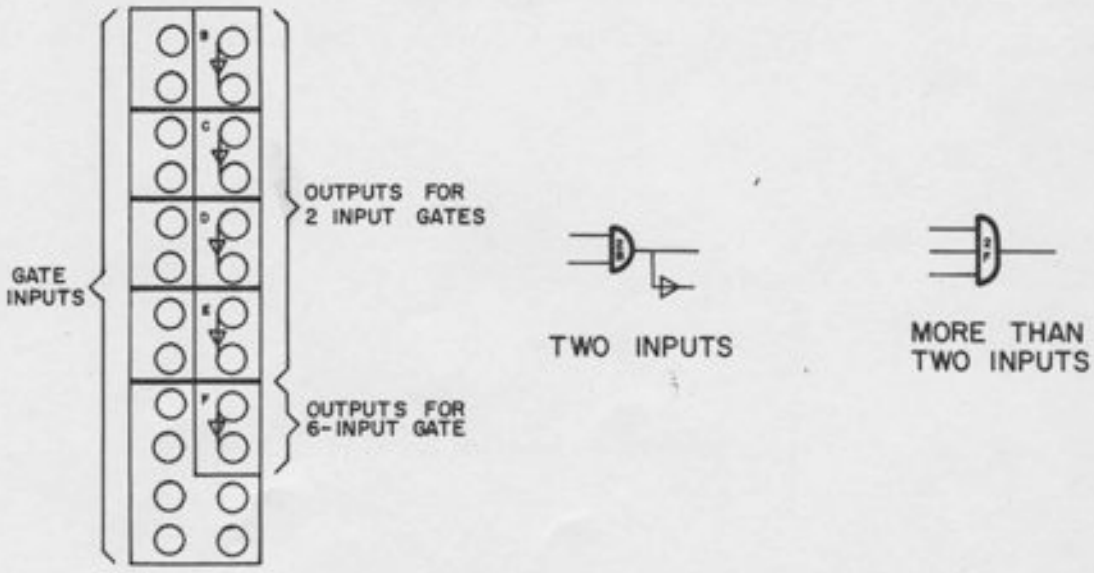


Figure 14.1. Patch Panel Terminations and Programmer's Symbols for AND Gates

14.2.1 The OR Function

Although there are no OR gates available as such, it is common practice to program OR gates where required. De Morgan's Theorem allows the use of AND gates to perform the OR function. Figure 14.2 illustrates the technique.

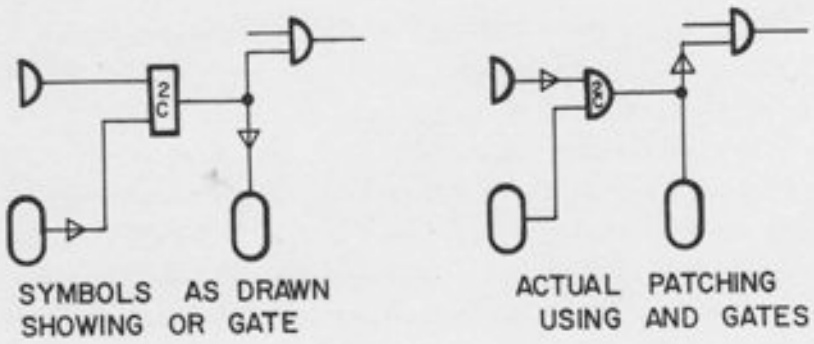


Figure 14.2. Using an AND Gate for the OR Function

14.2.2 Buffering

In case a signal must drive an extremely large load, the signal may be patched to a single AND gate input. The AND gate output may then be used to drive the load. This use is rare, since all logic outputs on the patch panel have sufficient driving capability for almost any load likely to be encountered in practice.

14.2.3 Inversion

A single-input gate may also be used as an inverter, to provide the complement of an output that does not have the complementary output terminated.

14.2.4 Display

Any logic signal that does not have an indicator (such as a logic trunk line) may be patched to an AND gate if visual display is desired.

CHAPTER 15

THE GPR TRAY

The GPR (General-Purpose Register) contains 4 flip-flops and the necessary logic to allow these flip-flops to be used as a four-bit shift register or counter. The four flip-flops may also be used as independent flip-flops, by simply ignoring the register control terminals.

15.1 LOCATION AND ADDRESSING

Each field contains *one* GPR tray, to the right of the integrator control tray (Figure 15.1). Hence, the entire computer contains 6 GPR's, or a total of 24 flip-flops. If the flip-flops are used together as a register, the register is addressed simply by the address of the field (0 through 5). Individual flip-flops are distinguished by the letters A, B, C, D. Thus a complete address for a single flip-flop consists of a number (0 through 5) and a letter (A-D), e.g., 0B, 3C, etc.

15.2 REGISTER INPUTS AND OUTPUTS

The inputs and outputs that refer to the register as a *whole* are as follows:

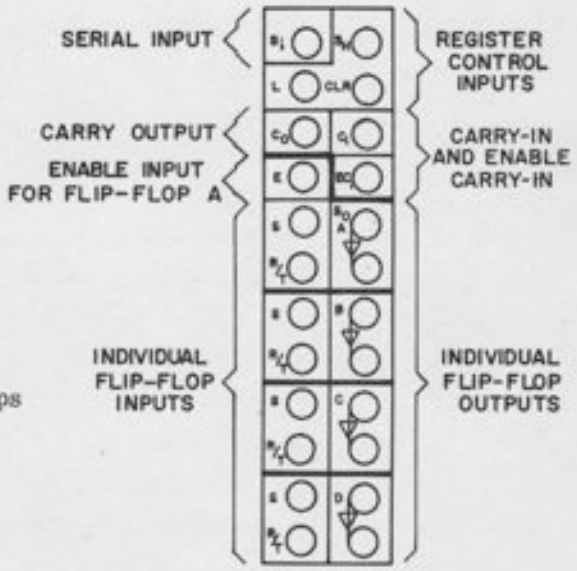


Figure 15.1. Patch Panel Terminations for a General-Purpose Register

15.2.1 CLR (Clear)

When this input is brought high, all four flip-flops in the register are cleared (reset). The CLR input is normally low if unpatched.

15.2.2 L (Load)

When this input is brought high, each flip-flop is set or reset by the individual flip-flop inputs on the patch panel. This feature allows parallel loading of the register from another register, or from any four signals on the patch panel. It is normally *high* if unpatched, so that by simply ignoring the "L" terminal and the other register control terminals, the flip-flops may be used independently.

15.2.3 SH (Shift) and SI (Serial Input)

When the SH terminal is high, the register shifts once on every clock pulse. The shift is from D to A; i.e., the bit in flip-flop D is shifted to C, the bit in C is shifted to B, and the bit in B is shifted to A. The bit at the SI (serial input) terminal is shifted into D. This feature allows cascading of shift registers. For example, an eight-bit shift register may be obtained by patching the SI of one register from the SO (Serial Output) of another. The SO of a register is simply the output of its "A" flip-flop.

A *ring shift register* may be obtained by patching SO to SI; in this mode of operation, the bit-pattern in the register is "shifted around in a ring," or "rotated". After four shifts, a four-bit ring shift register contains the same bit pattern it started with.

Note that the shifting, for either a regular shift register or a ring shift register, takes place once on *each* clock pulse during which the "SH" input is high. If the "SH" input is a blip (a synchronized pulse one clock period in length) it will cause a one-stage shift; if the "SH" input remains high for several clock intervals, the register will continue to shift at clock frequency as long as "SH" is high. When unpatched, the "SH" input is normally low, so that it does not interfere with the use of the register as a counter, or as four independent flip-flops.

15.2.4 CI and ECI (Carry-In and Enable Carry-In)

These terminals control the *counting* of the register. When used as a counter, the register increments once on *each* clock pulse during which CI = 1. If "CI" is a blip, it will cause the counter to increment by one. If CI remains high for several clock intervals, the counter will increment once on each clock pulse during which CI = 1. When unpatched, CI is normally low, so that it does not interfere with the use of the counter as a shift register or as four independent flip-flops. When the register is used as a counter, the "A" flip-flop is the least significant bit.

The ECI (Enable Carry-In) input provides a means of "blocking" or inhibiting the counting operation.

The CI and ECI inputs are connected to an AND gate internally, so that counting takes place only when *both* are high. However, the ECI input (unlike the CI input) is normally *high* if unpatched. Hence, if the programmer ignores the ECI input and patches only to the CI input, the counter will behave normally, as described above. However, a logic signal patched into ECI will *prevent* counting when it is *low*. Thus the ECI terminal exercises a sort of "mode control" over the counter; when ECI = 0, the counter may be thought of as being in the *hold* mode - it will not count, even if CI = 1.

15.2.5 CO (Carry Out)

The Carry-out signal is high whenever the register contains the number fifteen (1111 in binary notation) *and* CI = 1. This signal may be used to "extend" the counter - for example, if CO is patched to CI of another counter, an eight-bit counter results. Note that CO is effected by CI, but *not* by ECI.

15.3 FLIP-FLOP INPUTS AND OUTPUTS

In addition to the register inputs and outputs, there are inputs for the individual flip-flops.

15.3.1 S (Set) and R (Reset)

The set and reset inputs determine the behavior of the flip-flop as follows:

1. When S = 1 and R = 0, the flip-flop sets (its output becomes ONE) on the next clock.
2. When S = 0 and R = 1, the flip-flop resets (its output becomes zero) on the next clock.
3. When S = 0 and R = 0, the flip-flop output remains constant, i.e., it "remembers" or "holds" its previous state.
4. When S and R are both ONE, the flip-flop "triggers" (changes state) on the next clock.

If unpatched, the S and R inputs are normally low.

15.3.2 Triggering

As pointed out above, in Paragraph 4, the flip-flop will trigger if both S and R are at logic ONE. The "SET" input, if unpatched, is connected to the RESET input by normally-closed patching contacts. Hence, if a signal is patched to the "RESET" input only, it will function as a trigger input. Note that the "RESET" input on the patch panel is labeled "R/T" (RESET or TRIGGER) to indicate its dual function. Of course, if logic signals are patched to both R and T, the connection between the two is broken.

15.3.3 The "E" (Enable) Input

The "A" flip-flop in each GPR is provided with an Enable input. This input, when low, prevents the flip-flop from changing state in response to its SET and RESET inputs. Thus, the Enable input exercises a sort of "mode control" over the flip-flop. If the "E" input is left unpatched, it is normally high, and the flip-flop behaves normally. The enable input is useful for such applications as "sampling" a digital signal at a certain time, or for inhibiting a logic program from operating while some other logic program is in progress.

Only the "A" flip-flop has an enable input. However, the "L" input may be used as a "group enable" if desired. The internal connections between the "L" and "E" inputs are shown in Figure 15.2.

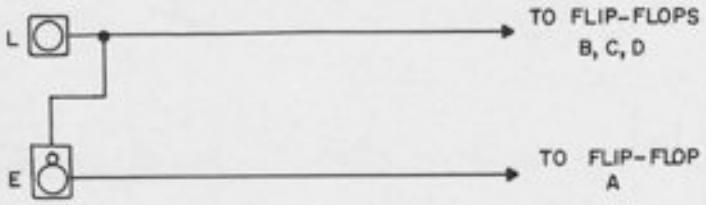


Figure 15.2. Internal Connections for the "Load" and "Enable" Inputs

The reader should be able to verify the following facts from the figure:

1. If L and E are left unpatched, then all four flip-flops respond to their S and R inputs all the time. (Remember, "L" is normally high). This is the most common mode of operation.
2. If "L" is left unpatched and a logic input is patched to "E", then flip-flop A is enabled by the "E" input, while flip-flops B, C, and D operate normally (they respond to their "S" and "R" inputs all the time). This is the second most common mode of operation.
3. If "E" is left unpatched, and a logic input is patched to "L", the "L" input acts as a "GROUP ENABLE" input. All four flip-flops respond to their "S" and "R" inputs only when L = 1. This mode of operation is quite rare when the four flip-flops are used independently. The "L" terminal is used primarily when the flip-flops are used together as a four-bit register.
4. If both "E" and "L" are patched to logic inputs, then the "E" terminal enables flip-flop A and the "L" terminal enables flip-flops B, C, and D. This mode of operation is quite rare, but occasionally comes in handy when several flip-flops have to be enabled from a common signal.

15.4 PROGRAMMER'S SYMBOLS

Programmer's symbols for an individual flip-flop and for a register are given in Figure 15.3. Note that when the unit is used as a *register*, the "A" bit is drawn on the *right* and the "D" bit on the *left*. If this convention is understood, the lettering "D, C, B, A" inside the register symbol may be omitted. The reason for drawing the "A" bit on the right is that it is the least significant bit in counting. Hence, this order corresponds to the usual method of writing numbers, with the most significant digit on the left, and the least significant on the right. For consistency, the register should be drawn the same way, even if it is used as a shift register, rather than as a counter. The shift is from D to A, i.e., from left to right.

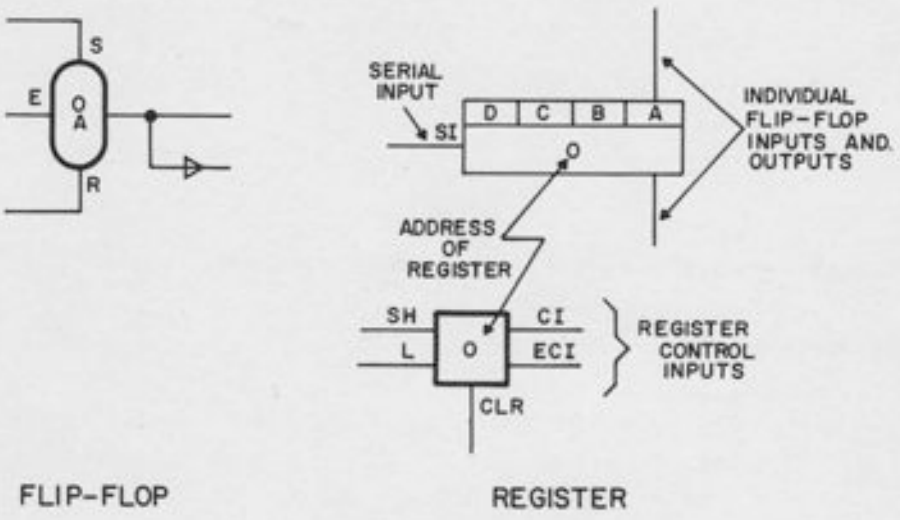


Figure 15.3. Programmer's Symbol for a Flip-Flop and a Register

15.5 DISPLAY AND MANUAL CONTROL

Each flip-flop in each register is displayed on an indicator light on the logic readout panel. These lights are also pushbuttons, allowing flip-flops to be set and reset manually. See Paragraph 2.3.5 for details.

CHAPTER 16

THE BCD COUNTER TRAY

16.1 LOCATION AND ADDRESSING

The 680 logic section has provision for three counter trays (Figure 16.1), in fields 1, 3, and 5. Each counter is a two-digit BCD (binary-coded decimal) counter capable of counting from 0 to 99. Two counters may be cascaded to count to 9,999, and three cascaded counters can count to 999,999. Each counter is addressed by the number of the field in which it appears, e.g., counter 1, counter 3, and counter 5. The counter may count either up or down.

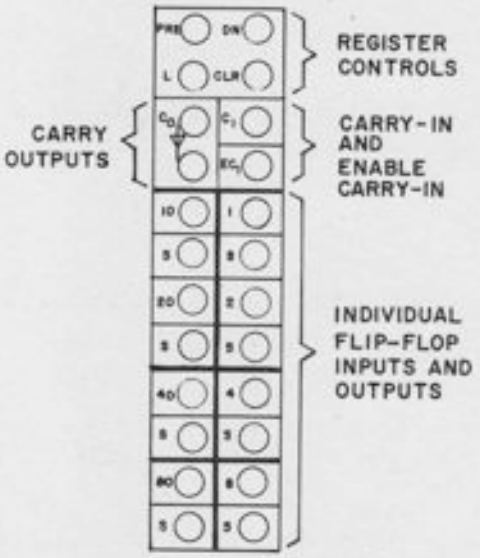


Figure 16.1. Patching Terminations for BCD Counter

16.2 READOUT AND MANUAL CONTROL

For each counter, there are two thumbwheels and two rows of pushbutton/indicators on the logic control panel. The thumbwheels are somewhat analogous to an "IC pot" for an integrator. They may be set manually to any value from 0 to 99. When the "PRE" terminal on the patch panel becomes high (logic ONE) the number on the thumbwheels is loaded into the counter.

The indicators display the contents of the counter at any time. By simply adding the numbers on all lights that are lit, the operator may determine the contents. For example, if the "40", "10", "2" and "1" lights are lit, the counter contains the number 53 (=40 + 10 + 2 + 1). Similarly, the operator may load any number from 0 to 99 into the counter manually, since the indicators are also pushbuttons. A CLEAR button at the bottom of each column allows all four flip-flops (corresponding to a single digit) to be cleared manually.

To load a given number manually into the counter, first clear both columns, and then press the appropriate pushbutton/indicators to set the corresponding flip-flops. It is *not* sufficient to pick flip-flops whose total "value" as indicated on the lights adds up to the required number. Each digit must be treated *separately*. For example, if it is desired to load the number 32 into the counter, the combination 20 + 8 + 4 is not correct, even though the sum is 32. The correct breakdown is 20 + 10 + 2, since the total in the "tens" column is 30, and the total in the "units" column is 2.

16.3 REGISTER TERMINATIONS

Even though some individual flip-flop inputs and outputs are terminated on the patch panel, the counter is not intended for use as eight independent flip-flops. Hence, the most important terminals are the ones that apply to the counter as a whole. These terminals are located at the top of the tray, and function as follows:

16.3.1 PRE (Preset)

When this terminal is high (logic ONE) the counter is set to the value on the thumbwheels on the next clock pulse. When PRE = 0, the thumbwheels have no affect on the counter.

16.3.2 DN (Down)

This terminal determines the *direction* of the counting. When it is high, the unit functions as a down counter; when it is low, the unit functions as an up counter. Note that it is the CI input which actually causes the counter to count; on each clock pulse for which CI = 1, the counter will either increment (if DN = 0) or decrement (if DN = 1). When CI = 0, no counting takes place, regardless of the DN input.

The DN input is normally low (if unpatched) so that the unit is normally an up counter. A pin in the DN terminal acts as a logic ONE; it makes the unit act as a down counter. If the DN terminal is patched from a logic signal, the counter becomes a bi-directional counter, capable of counting in either direction under control of the DN input.

16.3.3 CLR (Clear)

When this input becomes high, the counter is cleared (all flip-flops are reset) on the next clock.

16.3.4 L (Load)

When this input becomes high, the register is loaded from the patch panel inputs. A SET ("S") input is provided for each flip-flop, but no RESET input. The SET input is inverted internally

to drive the RESET input, so that, when L = 1, each flip-flop will be set (if its S input = 1) or reset (if its S input = 0). This input is normally low if unpatched.

16.3.5 CI and ECI

These input terminals function in the same manner as the corresponding terminals on a GPR. When CI = 1, the unit will count (either up or down, depending on the DN input) on each clock pulse. The ECI input, when low, blocks the CI input and prevents counting. The ECI input has no effect on the CO output. CI is normally low, and ECI is normally high. For a fuller description of these terminals, see Paragraph 15.3.4.

16.3.6 CO (Carry Out)

This output terminal is high whenever the CI input is high and the counter has reached its extreme value in the direction of counting. More specifically, CO is high whenever CI is high and one of the following conditions holds: either the DN input is high and the counter contains the number zero, *or* the DN input is low and the counter contains the number 99. Symbolically, this may be written as follows:

$$CO = CI \cdot (DN \cdot 00 + \overline{DN} \cdot 99)$$

The CO output may be used to cascade counters by patching the CO of one to the CI of the next.

16.4 INDIVIDUAL FLIP-FLOP TERMINALS

Each of the eight flip-flops in the counter has an individual SET input on the patch panel, but no reset input. The output is terminated, but not the inverted output. The flip-flops are not intended to be used independently, but the input terminals are convenient for loading the register from logic signals, and the output terminals allow decoding of the flip-flops to determine when a given state has been reached.

16.5 PROGRAMMER'S SYMBOL

A programmer's symbol for a BCD counter is given in Figure 16.2. Only those inputs that are actually patched need be drawn.

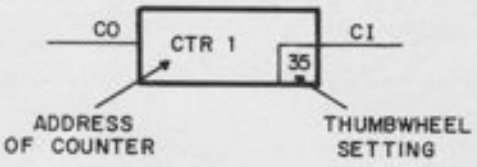


Figure 16.2. Programmer's Symbol for BCD Counter

CHAPTER 17

THE MONO/DIFF TRAY

The mono/diff tray contains three monostable timers and three differentiators. The patch panel terminations for the mono/diff tray are shown in Figure 17.1.

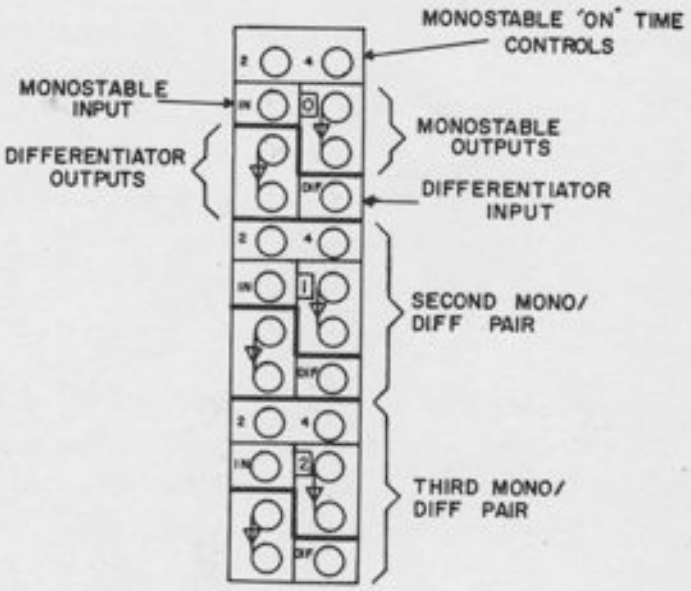


Figure 17.1. Patch Panel Terminations for Mono/Diff Tray

17.1 LOCATION AND ADDRESSING

The 680 contains two mono/diff trays; a total of six monostable timers and six differentiators. These trays are in fields 0 and 4, to the left of the interface trays. Within a tray, the monostable timers and differentiators are numbered 0, 1, and 2. Hence, a complete address for a monostable or a differentiator consists of two digits; one for the field and one for the individual component, e.g., monostable 01 or differentiator 42.

17.2 THE MONOSTABLE TIMER

The monostable timer is a device that produces an output pulse of fixed duration whenever its input signal becomes high. The pulse duration, also called the period, is adjustable by the programmer. On the 680, the period may be as short as 1 microsecond or as long as 100 seconds.

Monostable timers are generally used in applications where precise setting of the delay time is not crucial. Such applications include putting a track/store unit momentarily into *track* mode long enough to allow it to track a new value, (about 10 microseconds), stopping a logic program until a relay has time to close (about 1 millisecond) or stopping or delaying an analog program until the pen on an X-Y plotter has time to be raised or lowered (about 150 milliseconds). For such applications, the period does not have to be accurate to better than about ±10%. The period on the 680 monostable timer may be set to within ±1/2%. If more precisely timed intervals are desired, a counter should be used.

When the logic input to the monostable becomes high, the output becomes high on the next clock pulse, and remains high for a predetermined period. While the monostable output is in the "high" state, the unit is completely insensitive to its logic input; the input may remain high or become low again, but the output remains high for the duration of the predetermined period. When the period is over, the output becomes low, and the monostable again becomes sensitive to its input. If the input is still high, the output becomes high again for another full period.

17.2.1 Determining the Period

The period of the monostable is determined by the two input terminals marked "2" and "4" at the top of the monostable patching area, and by manual controls on the logic readout panel (see Paragraph 2.3.3). The logic inputs determine the general range of values, and the manual controls determine the actual setting within that range. The ranges are as follows:

"4" Input	"2" Input	Range
0	0	1 - 100 Microseconds
0	1	100 Microseconds - 10 Milliseconds
1	0	10 Milliseconds - 1 Second
1	1	1 Second - 100 Seconds

Note that each range is 100 - 1; that is, the longest interval is 100 times the smallest. Note also that each range is 100 times longer than the preceding range, so that the lower end of one range coincides with the upper end of the preceding range. In the actual unit, the ranges are slightly greater than those given in the table, so that there is enough overlap to assure that any value in the range may be set.

The value within the range is determined by the controls on the logic readout panel. These controls consist of a ten-digit thumbwheel and a vernier pot (see Figure 2.2).

The "2" and "4" terminals may be patched either with pins or with logic inputs. A pin acts like a logic ONE; if unpatched, these inputs are normally low.

17.2.2 Programmer's Symbol

A programmer's symbol for the monostable timer is given in Figure 17.2. The period is written in the small box at the top of the symbol, or it may be written on the assignment sheet.

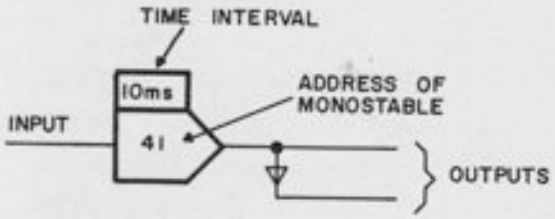


Figure 17.2. Programmer's Symbol for Monostable Timer

Figure 17.3. Programmer's Symbol for Differentiator

17.3 THE DIFFERENTIATOR

A differentiator produces an output blip (a synchronous pulse one clock period long) whenever its input changes from 0 to 1. The output becomes high on the same clock pulse on which the input does; it becomes low one clock period later. A programmer's symbol for the differentiator is given in Figure 17.3.

CHAPTER 18

MISCELLANEOUS LOGIC COMPONENTS

The strip area beneath the logic row contains a number of miscellaneous terminations, most of which are connections to external devices.

18.1 TRUNKS

There are 18 logic trunks, arranged in 3 groups of 6. They are numbered 00-05, 10-15, and 20-25. They may be used to trunk signals between computers, or between a computer and some external device.

18.2 SCOPES, PLOTTERS, AND RECORDERS

Beneath logic field 5 are controls for lowering the pens on X-Y plotters, triggering sweeps on oscilloscopes, and changing the chart speed of a strip-chart recorder. Beneath the interface tray in field 2 and the integrator control tray in field 3 are inputs for an oscilloscope to display logic signals, and ERASE inputs for use with a storage scope.

18.3 DIGITAL PUSHBUTTONS

Six general purpose pushbuttons are terminated in the strip area. They are numbered 0-5. The outputs may be set high or low by pushing buttons on the logic readout panel. The output may be either a level or a blip, at the discretion of the programmer. A programmer's symbol for a digital pushbutton is shown in Figure 18.1. See Paragraph 2.3.3 for details.

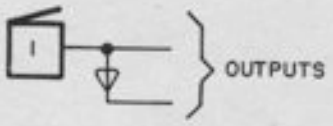


Figure 18.1. Programmer's Symbol for Digital Pushbutton

CHAPTER 19

ANALOG TIME SCALE CONTROL

Analog time scale control is provided, which allows an entire problem or parts of the problem to be sped up by a factor of 10 or 1000 (or both). The master computer time scale is under the control of four pushbuttons on the control keyboard marked "N" and "F" (a mutually-exclusive pair) and "SEC and "MS" (another mutually exclusive pair). At any given time, one selection from each pair is in force.

The normal selection is "N" (Normal) and "SEC" (Seconds). This gives every integrator (except those that have different control patched individually) a standard (10 microfarad) capacitor. The time constant of the integrator, with the standard "gain 1" resistor (100K) is one second.

Selecting "MS" (Milliseconds) provides a 1000:1 speedup by reducing the integrating capacitors; the time-constant for a "Gain 1" input becomes one *millisecond.*

Selecting "F" (Fast) instead of "Normal" reduces the effective time constant to 0.1 second or 0.1 milliseconds, providing a 10:1 speedup. Note that when both "F" and "MS" are chosen, the speedup is 10,000:1, relative to the "Normal Seconds" selection.

The time scale selection for the computer may be made by logic signals as well as by pushbutton. This feature allows, for example, automatic iteration at high speed with results plotted at low speed, all under logical control. The master time scale inputs are located in the logic strip area beneath the mode control timer tray in logic field 2.

Figure 19.1 shows the relation between pushbutton control, patched master time scale control, and individual integrator control. The "F" button sets a flip-flop; the "N" button resets it. The flip-flop output determines the Fast/Normal selection for the computer through normally-closed contacts. Patching into the master "F" control terminal overrides the pushbutton control, and puts the "F" selection for the entire computer under control of the patched logic signal. Similarly, an individual integrator may be disconnected from the master computer control by patching.

In addition to the capacitor values the time scale selection also affects the timing intervals of the rep-op timer. However, the rep-op timer may also be separated from the master time scale selection if desired. See Chapter 20 for details.

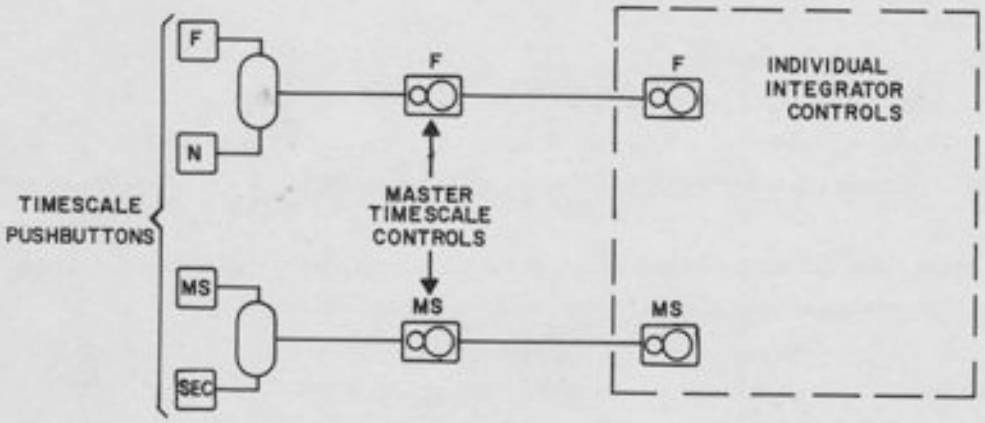


Figure 19.1. Master and Individual Time Scale Control

CHAPTER 20

ANALOG MODE CONTROL

20.1 MANUAL AND LOGICAL CONTROL

The analog mode selection may be made either manually or from patched logic signals. As mentioned in Paragraph 2.6.4, the mode control buttons include one marked "PP". When this is depressed, the mode is controlled from the logic area of the *patch panel*. The three modes *IC, hold,* and *operate* may be selected by logic. Control is returned to the pushbuttons by selecting any mode manually.

20.2 NORMAL REPETITIVE OPERATION

The 680 is provided with an extremely flexible and versatile rep-op timer for repetitive and iterative operation. However, many of its features may be ignored in ordinary rep-op, where the goal is simply to cycle the computer between *operate* and *IC*, and observe the results on an oscilloscope. Hence these features have been arranged so that they don't "get in the way" of the person who wants normal repetitive operation. Normal repetitive operation requires *no patching* in the mode control tray (in logic field 2). All that is necessary are the following steps:

20.2.1 Select the time scale desired. (Typically N, MS, since this gives a 1000:1 speedup; whatever takes place in one second when N, SEC is selected will now take place in one millisecond.)

20.2.2 Select the *operate* and *IC* times on the TIMER controls. These are thumbwheels in the upper left-hand corner of the analog readout panel. The two intervals may be set independently. The IC period is "A"; the OP period is "B". The "C" interval is not used in normal repetitive operation; it should be set to zero.

Each interval may be set to three digits. The actual interval duration depends on the time-scale selected -- the timer speeds up automatically as the time scale is increased. If constant interval duration, independent of time scale changes is required, it can be obtained by patching; see Paragraphs 20.3.1 and 20.3.2.

If "N" and "SEC" are selected, the wheels read directly in seconds, with the decimal point after the second digit; e.g., 23.4 seconds, 99.5 seconds, etc. If "N" and "MS" are selected, the wheels read in milliseconds (e.g., 23.4 milliseconds, 99.5 milliseconds).

The "F" selection shortens these intervals by a factor of ten, so that the above settings would correspond to 2.34 seconds (or milliseconds) and 9.95 seconds (or milliseconds).

20.2.3 After selecting time scale and setting the IC(A) and OP(B) intervals, depress the PP button. This transfers mode control to the rep-op timer, and also *starts* the timer. The timer begins with a full "A" (IC) cycle. To leave repetitive operation, select any other mode manually.

20.3 FUNCTIONS OF THE TERMINALS IN THE TIMER TRAY

The 680 mode control and rep-op timer terminals appear in the "MODE CONTROL/TIMER" tray in logic field (Figure 20.1). This section explains *what* each of these terminals does without explaining the actual circuit details. Block diagrams and a general discussion of the internal circuitry are given in Paragraph 20.4.

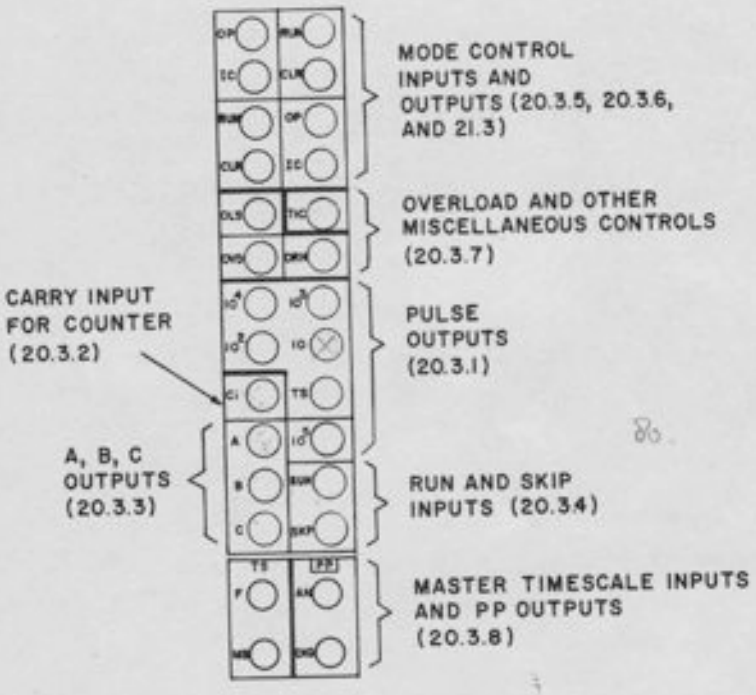


Figure 20.1. Mode Control/Timer Tray

20.3.1 Pulse and TS Outputs

These outputs are marked 10^5, 10^4, 10^3, 10^2, 10, and TS (time scale). At each of these outputs a series of pulses appear at regular intervals. The pulses are synchronized with the clock

and with each other; that is when any pulse output is high, all outputs of higher frequency are high also. Each pulse is a "blip", that is, a synchronized pulse one clock period in length. The outputs are labeled with the frequency in pulses per second. Thus, for example, 10^4 pulses per second appear at the 10^4 terminal, or ten pulses per millisecond.

The frequency of the TS (time scale) output is controlled by the time scale selection. It is 10 pulses per second for "Normal Seconds" selection, and speeds up in proportion: i. e., 100 pulses per second in "F, S" selection; 10,000 pulses per second in "N, MS" and 100,000 pulses per second in "F, MS".

NOTE

These pulses are present only when the rep-op timer is running.

20.3.2 The CI Input

The CI (Carry In) input is the input to a 3-decade counter. The counter counts from zero up to the appropriate number, as determined by the A, B, or C thumbwheels. For example, if "A" has been set to the digits 234, "B" to 995, and "C" to 312, then the timer will stay in the *A* mode until 234 CI pulses have been received, then switch to the *B* mode for a count of 995, then enter the *C* mode for a count of 312, and then return to the *A* mode for another count of 234. If the *C* mode is set to zero, it is skipped, the timer will simply cycle between A and B.

If nothing is patched into CI, then it is normally connected to the TS pulse output. This connection provides the timing intervals described in Paragraph 20.2.2. For example in "N, SEC" the TS frequency is 10 pulses per second. Hence it would take 23.4 seconds for the counter to reach a count of 234. In other time scales, the pulse rate is proportionally faster. However, any pulse rate may be patched in, instead of the normally-connected "TS" signal.

20.3.3 The A, B, C Outputs

These are logic outputs that tell which "state" the timer is in; at any given time, only *one* of these outputs is high. In normal rep-op, A is the *IC* mode, and B is the *operate* mode; however, these logic signals may be used for any purpose, not just for mode control.

20.3.4 RUN and SKP Inputs

The inputs marked RUN and SKP control the operation of the timer. When the RUN input is high, the timer runs normally, as described above. When the RUN input becomes low, the

timer is forced to the *A* mode, and stops there. When the RUN input becomes high again, the timer starts to operate again *starting with the "A" interval.*

NOTE

The "RUN" input that controls the timer is near the bottom of the tray above the SKP input. It should not be confused with the "RUN" input near the top of the tray, which serves as a logic mode control input.

If nothing is patched to RUN, it is normally connected to the PP logic signal (see Paragraph 20.3.8). Hence depressing "PP" not only transfers control of the mode to the patch panel, but starts the rep-op timer as well.

When the SKP input comes high, the timer skips to its next state, even though the full thumbwheel count has not been reached. If it is in A, it skips to B, if in B, it skips to C; from C, it skips to A. If C is set to zero, the SKP input will cause a skip from B to A.

The skip feature is useful for terminating a run by a condition other than time - for example, operating until a given analog variable crosses zero. The skip input responds only to a *rising* edge; if the skip input comes high and stays high, the timer will not skip again until the skip input becomes low and then high *again.*

20.3.5 IC, OP Inputs

These inputs control the computer mode according to the same truth-table that holds for an individual integrator:

IC Input	OP Input	Resulting Mode
1	ANY	IC
0	1	OP
0	0	HOLD

Note, however, that the IC and OP inputs have no effect on the computer mode unless the *PP* mode has been manually selected.

NOTE

In ordinary rep-op, without any patching, the OP output is high all the time. Repetitive operation is accomplished by raising the IC line during the "A" interval, since this overrides the "OP" signal. If output logic indications for the computer mode are required in rep-op, they should be taken from the A, B, C timer outputs, not the mode control outputs.

20.3.7 The Overload and TIC Terminals

These four terminals are located immediately below the mode control inputs and outputs. They function as follows:

1. OVD (Overload). This output signal becomes high whenever *any* component overloads. It is *not* synchronized with the clock.
2. ORH (Override Hold). This is an input terminal. When it becomes high (logic ONE) *every* integrator in the computer goes into the *hold* mode, regardless of local logic patching. This feature is useful for "freezing" a problem to locate a source of trouble - e.g., by patching OVD to ORH. If ORH is not patched, it is normally low; hence it has no effect.
3. OLS (Overload Store). When this input becomes high, the overload condition is stored; that is, the next time a component overloads, its light will *stay on*. The OVD logic indication and the audible alarm all remain on even after the overload condition is removed. This feature allows "trapping" of a transient overload that might otherwise come and go too fast to track down.
4. TIC (Track/Store IC). This is the master input which puts all track/store units in the *IC* mode. This input may, however, be overridden for any particular track/store unit by local patching.

20.3.6 IC and OP Outputs

These outputs sense the state of the computer at all times, either in manual operation, or repetitive operation. The output becomes high when the computer is in the corresponding mode. Both outputs are low in the *hold* mode.

20.3.8 TS and PP Terminals

These terminals are *below* the timer tray. The TS (time scale) terminals are *inputs;* they are explained in Chapter 19. The "PP" terminals are *outputs;* they indicate whether the analog and/or digital modes are under patch panel control, as opposed to pushbutton control.

20.4 CIRCUIT DETAILS

The block diagrams of the rep/op timer and mode control tray in this section are intended to give the interested programmer some indication of the circuitry involved and the logical operations performed. They are not intended to be complete enough for maintenance purposes.

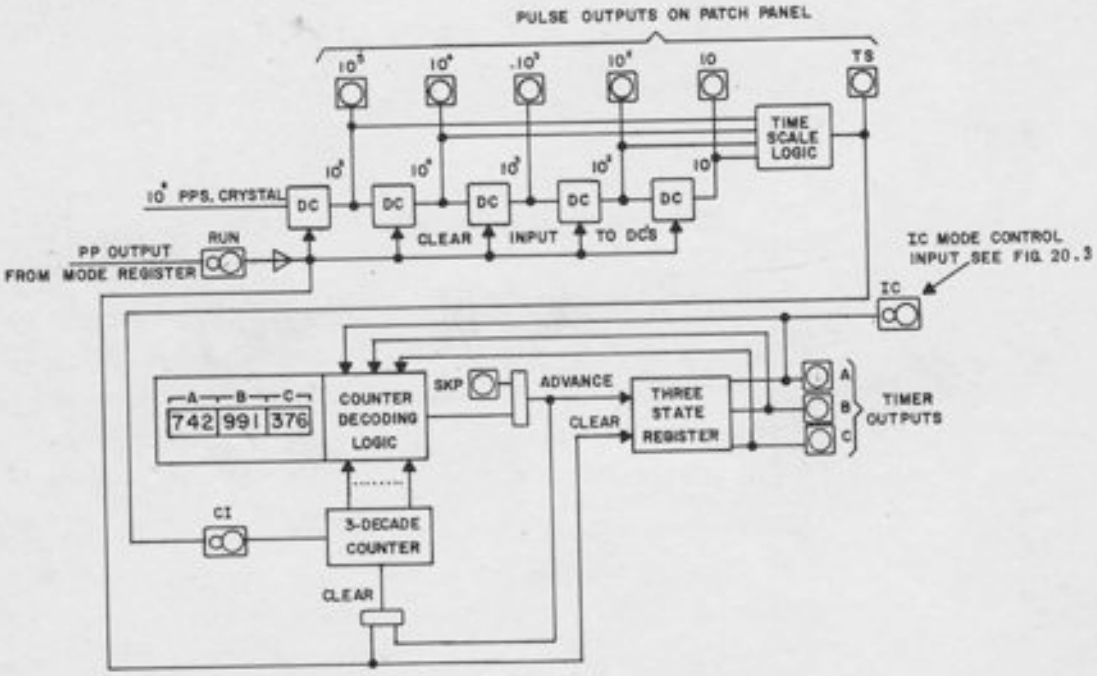


Figure 20.2. Timing Pulses and Rep-Op Timer

20.4.1 Timing Pulses and Rep-Op Timer

Figure 20.2 gives a general block diagram of the pulse sources and the rep-op timer. Starting at the upper left-hand corner, the input marked "10^6 pps crystal" comes from a crystal-controlled oscillator (10^6 pulses per second). This is the master clock source for the entire computer. It is fed into a "chain" of cascaded decade counters (marked "DC" in the figure). Each dc gives a pulse out after every ten pulses in; hence the frequency of each dc pulse output is ten times slower than that of the previous one. These pulse rates are terminated on the logic panel. The TS signal is obtained by appropriate gating of the pulses with the "F" and "MS" signals, to produce a pulse rate dependent upon the time scale selection.

The "TS" input is normally connected to the "Carry In" of the rep/op "timer" (which is really a counter). The "timer" consists of a 3-decade counter which can count from 000 to 999. It counts carry-in pulses until the number of pulses agrees with the thumbwheel setting for whatever mode the unit is in at the time. When the actual counter contents match the appropriate thumbwheel, the decoding logic generates an output signal which clears the counter and advances the 3-state register to the next state; from A to B, from B to C, or from C to A. (If the C thumbwheels are set to zero, the register advances from B back to A.)

The SKP input causes the same advancing of the three-state register and clearing of the 3-decade counter as would have occurred if the counter contents matched the thumbwheels. Hence the SKP allows a "skip" to the next state. The RUN input, when high, allows the unit to function normally; when it is low, it clears the decade counters generating the pulses, clears the 3-decade counter and clears the three-state register (i.e., forces it to the "A" state). The A, B, and C outputs appear on the logic panel and may be used for any purpose. Note that the "A" output is normally connected to the *IC* mode control input.

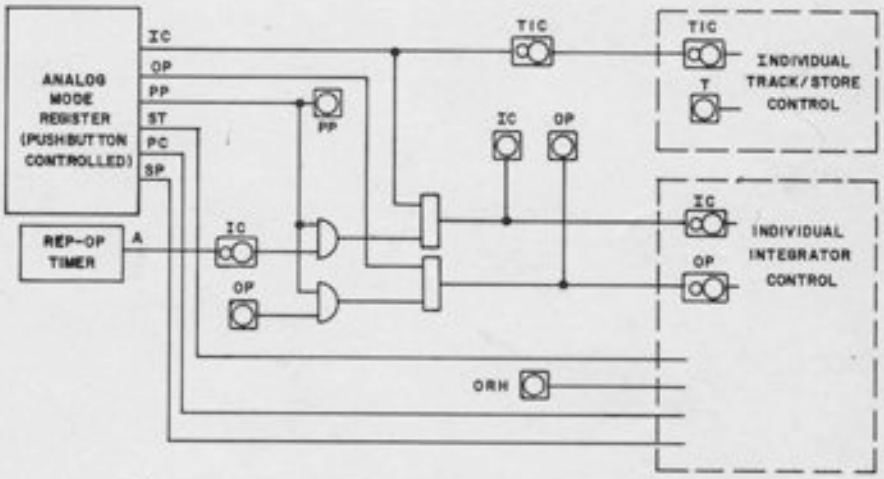


Figure 20.3. Mode Register and Mode Control Logic

20.4.2 Mode Register and Mode Buses

The Mode Register in Figure 20.3 "remembers" the manual mode selection. It has a different output line for each of the seven selectable modes (all but the *hold* mode are shown in the figure). Note that the master mode buses, which terminate on the logic panel and also are connected to each integrator control tray, can receive their signals either from the patch panel (if the "PP" output is high, the AND gates are enabled) or from the mode register (if the "PP" is low). These buses run to every integrator control tray. However, the use of normally-closed connectors permits the operator to "break the integrator away" from the main mode control by local patching. Also note that the SP, PC, ST and ORH (see Paragraph 20.3.7) enter each integrator control tray. These signals also operate independently of local patching.

CHAPTER 21

LOGIC MODE AND CLOCK RATE CONTROL

21.1 THE LOGIC MODES

The logic system has four modes, as follows:

1. Clear. In this mode, all flip-flops are cleared (set to zero) and remain at zero until the *run* mode is selected. Comparator outputs are not "cleared," but are held constant. This is somewhat analogous to the *IC* mode of an analog computer.
2. Stop. This is somewhat analogous to the *hold* mode on an analog computer. All flip-flop outputs (including those in comparators) are "frozen" but not cleared.
3. Run. In this mode, the logic operates normally.
4. PP (Patch Panel). In this state, control of the *run*, *stop* and *clear* modes is transferred to the input terminals on the logic panel (in the mode control/timer tray in logic field 2).

21.2 CLOCK RATES

The clock rates are as indicated on the control panel; 10^6, 10^5, 10 and STEP. The 10^6 clock rate is used for normal operation; there is only a microsecond of duration between clock pulses. The slower clock frequencies are useful mainly during checkout of a logic program. (The same is true of the STEP input.) When the *step* mode is entered, the clock stops as soon as the operator's finger leaves the button. Depressing the button a second time produces a short pulse (one clock period) in width, which allows "single-step" operation of the logic during check out.

21.3 LOGIC DIAGRAM

A logic diagram for the logic clock and mode control system is given in Figure 21.1. The manual pushbuttons are in groups of four; each group controls a register (called the clock rate register and the logic mode register in Figure 21.1). Each register has four outputs (not all shown in the figure), and each output becomes high when it is manually selected on the pushbuttons. The outputs from the clock rate register are gated with the corresponding pulses (see Paragraph 20.3.1). The "system clock" is obtained by ORing these outputs together; the output line which is high determines the clock rate.

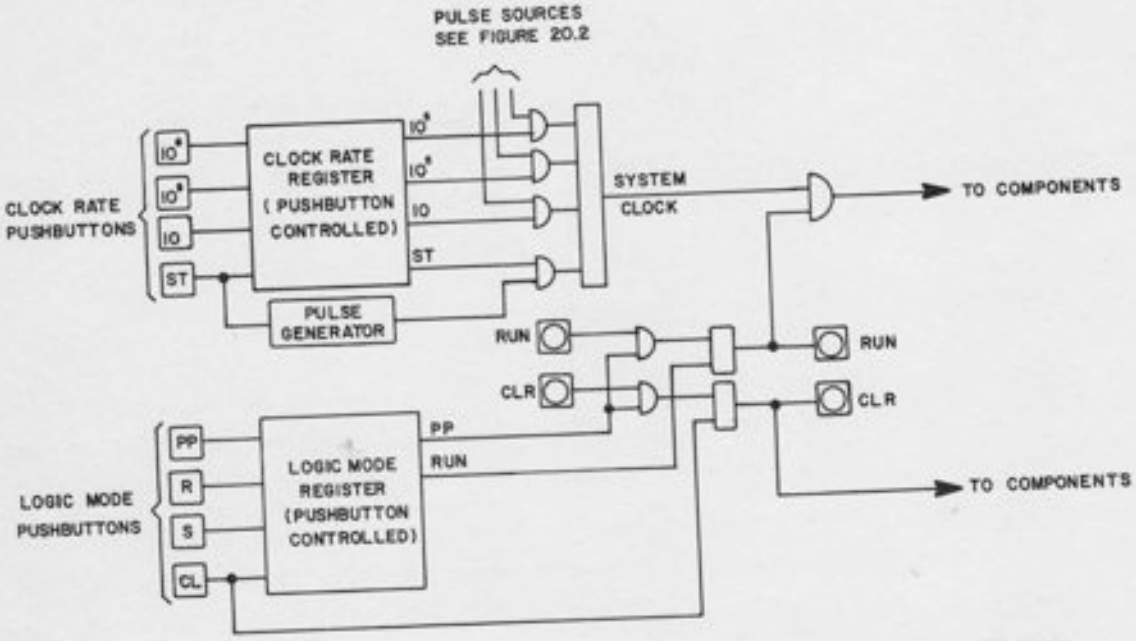


Figure 21.1. Logic Diagram of the Logic Mode and Clock Rate Control

The logic mode register operates in much the same way as the analog mode register. Note the AND and OR gates to drive the logic mode buses, allowing control from the patch panel or from manual pushbuttons. The *clear* mode pushbutton is momentary - the system is being cleared only while it is being held down. Once the button is released, the flip-flops remain cleared.

APPENDIX 1

ANALOG SYMBOLS AND PATCHING

This appendix contains programming information and patching diagrams for the analog components, but grouped by *application*, rather than by *component*. Detailed explanations of the internal circuity are omitted, more information on a component may be found in the chapter devoted to that particular component.

The layout of components on the 680 patch panel has been chosen to simplify both the symbols and the patching as much as possible. Thus, for many components, simplified (abbreviated) symbols are given for the more common modes of operation. By following certain conventions in assigning, drawing, and patching components, the programmer will find both the patch panel and the circuit diagram less cluttered.

1.1 INVERSION

Inversion may be performed with a Junction Inverter or with the output amplifier of an unused variable DFG. Of course, summers and combination amplifiers may also be used, but before doing this, the programmer should make sure he has enough of these amplifiers for integration, multi-input summation, track/store, and other such applications. Figure A1.1 gives the symbols for an inverter. It is recommended that inverters be drawn smaller than the summers and integrators, since only one input is needed. The input gain need not be shown if it is unity, which it usually is.

1.1.1 Inversion with Junction Inverter

To use the JI as a gain-one inverter, patch the input to the "1" terminal; the output appears at the three output terminals.

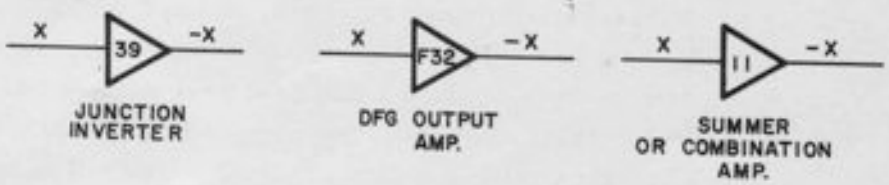


Figure A1.1. Programmer's Symbols for Inverters

1.1.2 Inversion with DFG Output Amplifier

Patch the input into the terminal below the x input on the left; the output appears at the two output terminals on the right. Be sure that the SLOPE MULTIPLICATION switch is in the "1" position for a gain-one inverter. Also, be sure that the amplifier is not being used with a DFG. If the 10/20 INV switch is in the INV position, both amplifiers in a pair are available as inverters. If it is in the "20" position, *only* the second amplifier in the pair (the one ending in -7) is available. If it is in the "10" position, then both amplifiers are used with 10-segment DFG's.

1.1.3 Inversion with Summer or Combination Amplifier

Patch as for a summer (see Paragraph 1.3), and patch the input to any of the "gain 1" input terminals.

1.2 INTEGRATION

The only component capable of integration is the combination amplifier. To use it as an integrator, a double-vertical plug is inserted into the control area as shown in Figure A1.2. The figure shows the IC input connected to the associated pot, this pot bears the same number as the integrator itself, and may easily be bottle-plugged to the IC input, and to ±Reference. Of course, any analog signal may be patched to the IC terminal, but, if a conventional IC pot is required, it is a good idea to use the associated pot.

1.2.1 Logic Symbols and Patching

For normal integrator operation, no patching is required in the logic area. For applications requiring individual mode control and/or capacitor selection, two mode control inputs (OP and IC) and two capacitor selection terminals (F and MS) are provided. These inputs, if used, should be drawn on the diagram in the sloping portion of the integrator symbol, as shown in Figure A1.2. A few special points are worth noting:

1. A pin in any of these terminals acts like a constant logic ONE. As an example of the use of pins, see Figure A1.3, which shows an integrator with a smaller than normal feedback capacitor. Such patching is useful in problems involving a wide range of time constants. The integrator in Figure A1.3 has a gain ten times that of the normal integrator. The "MS" button will speed this integrator up by a factor of 1000, just like a normal integrator, since the "MS" input is unpatched, and hence is still connected to the main mode control.

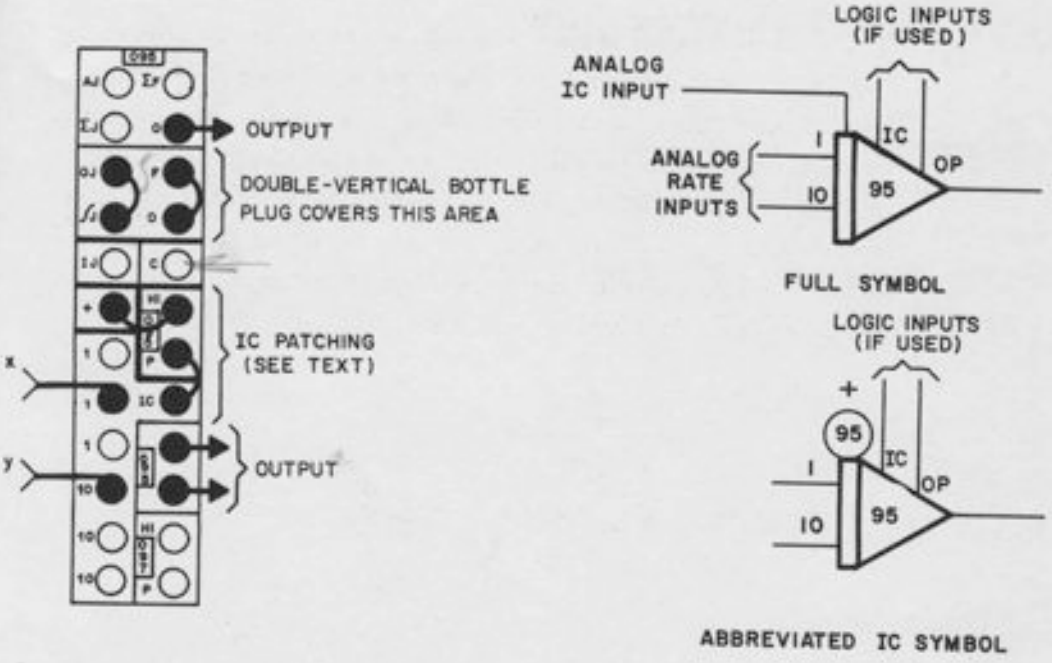


Figure A1.2. Standard Patching and Symbols for an Integrator

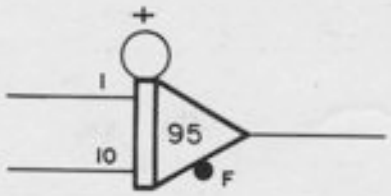


Figure A1.3. Integrator with Ten Times Normal Gain

2. IC/OP Mode Cycling. To cycle an individual integrator between the *IC* and *OP* modes under control of a logic input, the simplest connection is the one shown in Figure A1. 4. It is necessary to patch *something* into both the IC and OP terminals, if they are to be completely disconnected from the main computer mode. The connection in Figure A1. 4 is based on the fact that the IC input "overrides" the OP input - if both are high, the integrator is in the *IC* mode. Inserting a pin into the "OP" terminal assures that it is always high regardless of the main computer mode. The logic input is patched to the "IC" terminal; when it is high, the integrator is in *IC*, and when it is low, the integrator is in *operate*.

3. If mode control inputs are patched, it is not necessary to label them "IC" and "OP" provided the programmer follows the convention of drawing the IC logic input closer to the IC analog input. This rule helps prevent cluttering the diagram with unnecessary lettering. As an example, consider the circuit in Figure A1. 5. This figure shows an abbreviated symbol for the circuit in Figure A1. 4. The logic input closest to the IC pot is assumed to be the IC input; hence, the other one is the OP input. If capacitor selection logic inputs are used, they should be explicitly labeled: "F" and "MS".

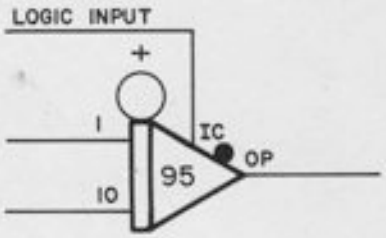


Figure A1.4. Integrator with IC/OP Mode Cycling from a Single Logic Source

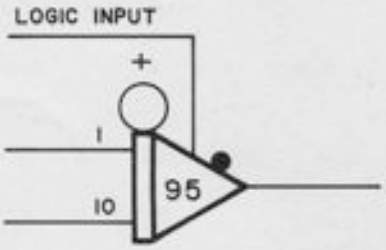


Figure A1.5. Abbreviated Symbol for the Integrator in Figure A1.4

1.3 SUMMATION

Summation may be performed with either type of summer, (the track/store summer or the limit summer) or with a combination amplifier. It is also possible to use a Junction Inverter as a summer by patching additional input resistors to its AJ, but this should rarely be necessary. Figures A1. 6, A1. 7, and A1. 8 show patching and symbols for the use of the track/store summer, the limit summer, and the combination amplifier. Note that in every case, a double-vertical plug is inserted in the top of the tray. No other patching is necessary except the patching of inputs and outputs.

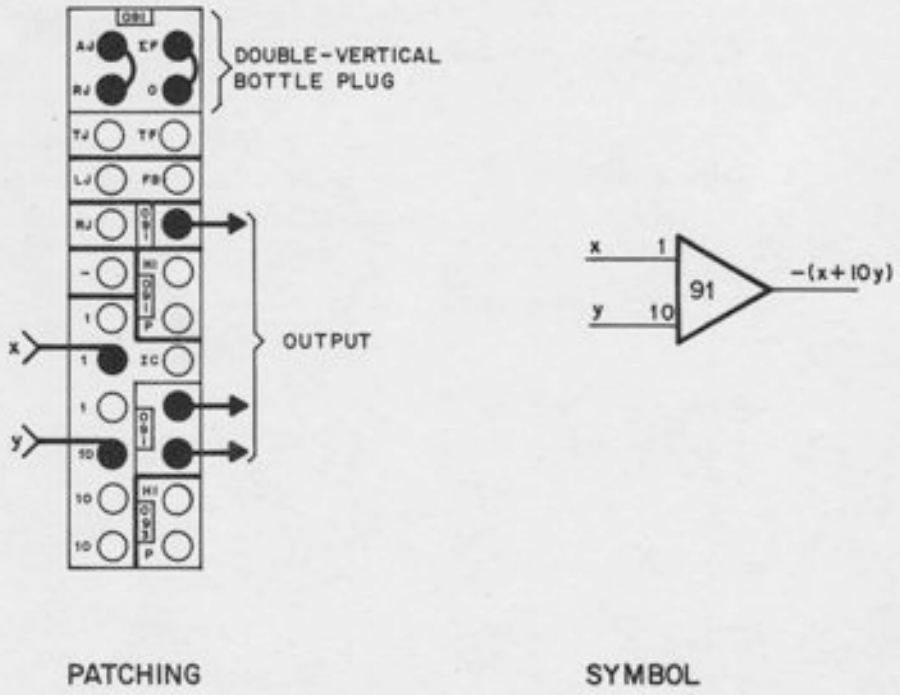


Figure A1.6. Summation with a Track/Store Summer

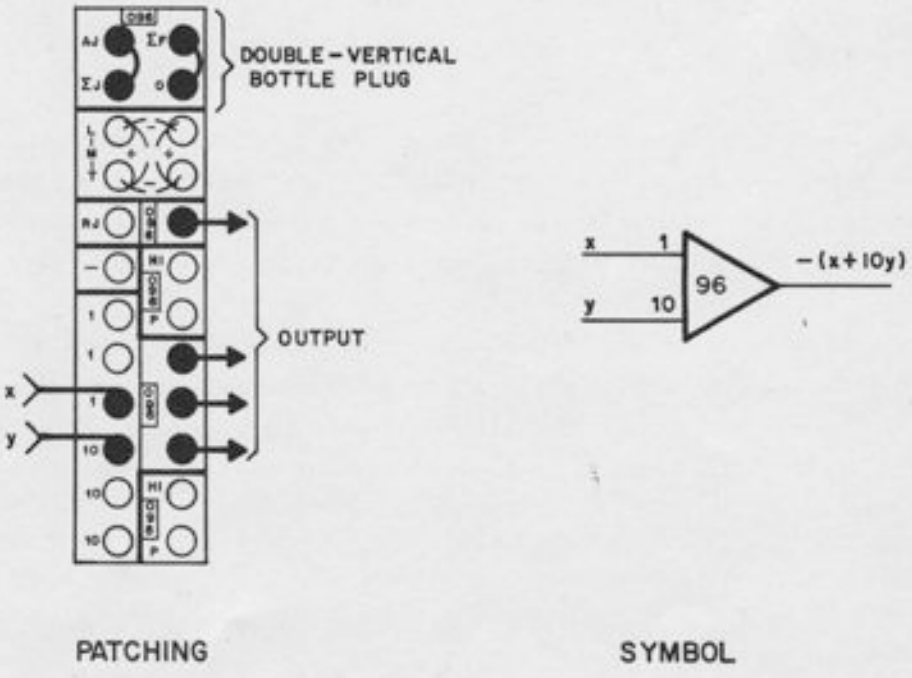


Figure A1.7. Summation with a Limit Summer

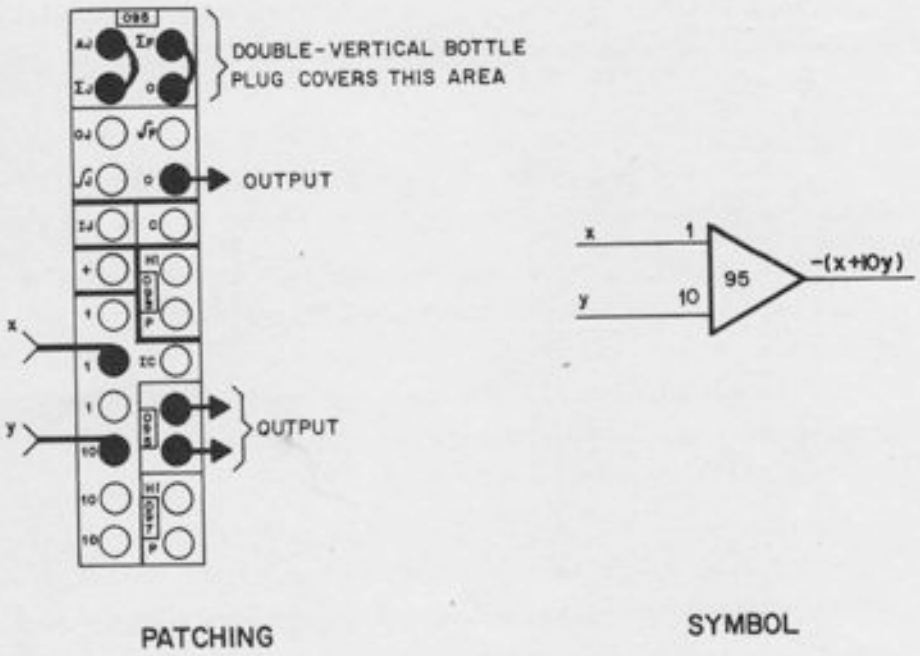


Figure A1.8. Summation with a Combination Amplifier

1.4 POT FEEDBACK

When a pot is used in the feedback path of a summer, the output is divided by the pot-setting. The pot attenuates the output signal before it is applied to the feedback resistor. The effect of the pot is to provide less feedback current for a given output voltage, which is equivalent to an increase in the effective feedback resistance, and hence an increase in gain.

Pot feedback has two main areas of application; obtaining large gains, and isolation of parameters. With "gain 10" input resistors and a pot-setting of 0.0100 in the feedback path, a gain of 1000 may be produced. Such gains are rarely necessary; the appearance of such a large gain is usually an indication of poor scaling. However, there are occasionally cases where such gains *are* necessary, even with proper scaling. For example, if two nearly equal signals must be subtracted, a large gain is required to obtain proper scaling for the difference.

The more common use of pot feedback is for parameter isolation. If it is necessary to multiply or divide the sum of many terms by a constant factor, this factor may be put on one pot in the feedback path, rather than on several input pots.

Figures A1.9, A1.10, and A1.11 show the use of the track/store summer, the limit summer, and the combination amplifier in pot-feedback applications. The following points should be noted:

1. Any input resistor may be used. If a "gain 10" resistor is used, for example, the output becomes -(x+10y)/10a. The "ΣF" terminal is used in the diagrams because this is the terminal normally used for feedback in the regular summer connection.
2. Any pot may be used. Unless there is a strong reason to do otherwise, it is recommended that the feedback pot should be the one with the same number as the amplifier. Note that if a pot is used which is *not* terminated in the same tray as the amplifier, it is necessary to patch the amplifier output to the pot input. This is not necessary in the circuits shown, because the amplifier output is connected to the pots in the same tray through normally-closed contacts. (See Chapter 8.)
3. The limit summer is shown with nothing patched in the LIMIT patching area. However, a LIMIT connection may be used if desired (see Paragraph 1.7). Similarly, the track/store summer is shown in normal summer operation in Figure A1.9. When it is used as a track/store unit, pot feedback is still possible; see Paragraph 1.5.1.

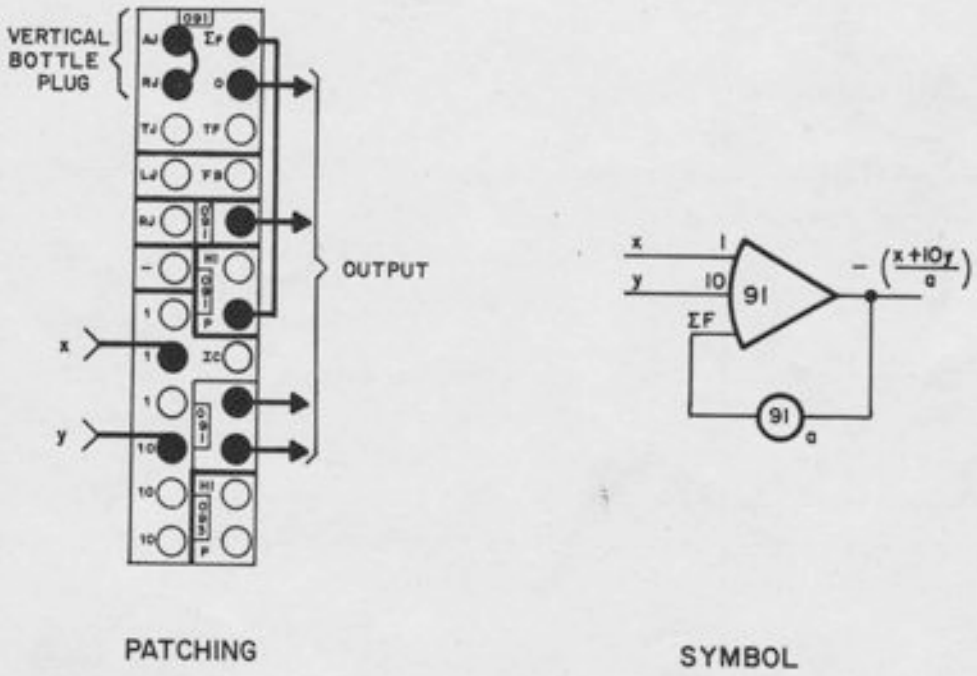


Figure A1.9. Using the Track/Store Summer with Pot Feedback

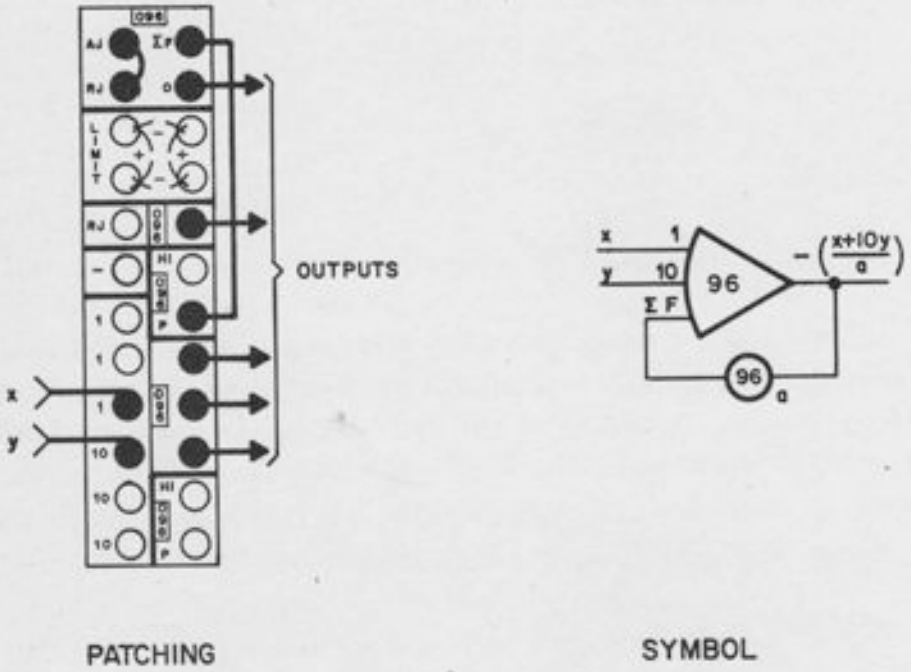


Figure A1.10. Using the Limit Summer with Pot Feedback

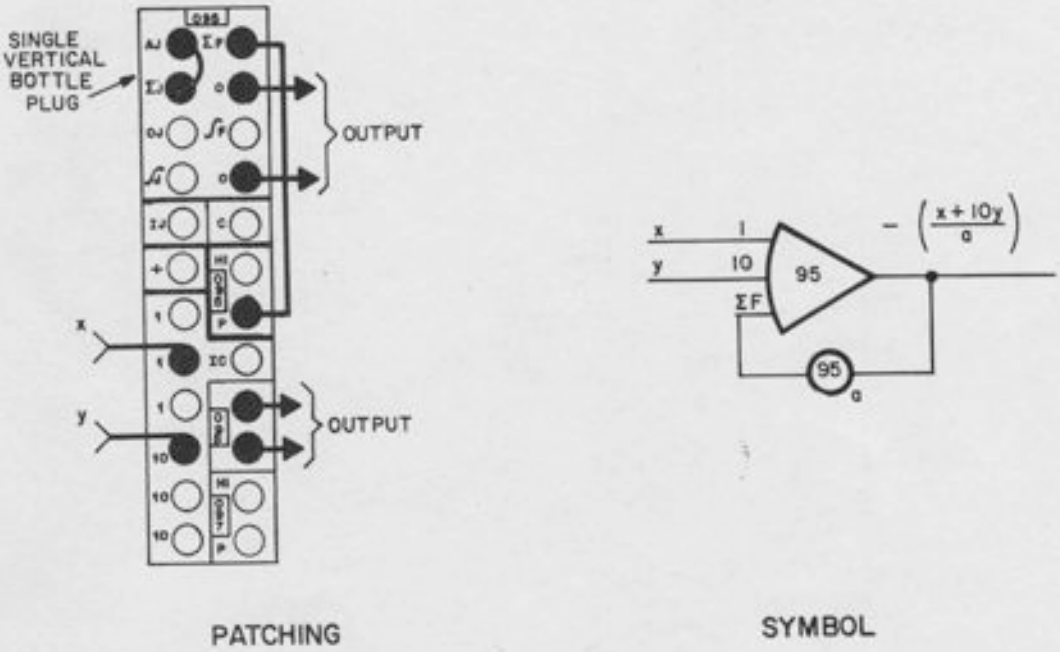


Figure A1.11. Using the Combination Amplifier with Pot Feedback

1.5 TRACK/STORE OPERATION

Track and store operation may be most conveniently performed with the track/store summer; however, the combination amplifier may also be used. The track/store unit offers the advantages of simpler patching, less tracking lag, and an *IC* mode. In addition, it is desirable to save the combination amplifiers for use as integrators.

1.5.1 Track/Store Unit - Conventional Feedback

The patching and programmer's symbol for a track/store unit with conventional feedback are given in Figure A1.12. When the unit is in the *track* mode, it behaves like a regular summer; the output is minus the sum of the inputs. In the *store* mode, the output is held constant. The *IC* mode allows an arbitrary initial condition to be established. If a pot is used for this IC, then, unless there is a good reason for doing otherwise, it is recommended that the associated pot be used - the one with the same address - since this allows bottle-plug patching of the IC input.

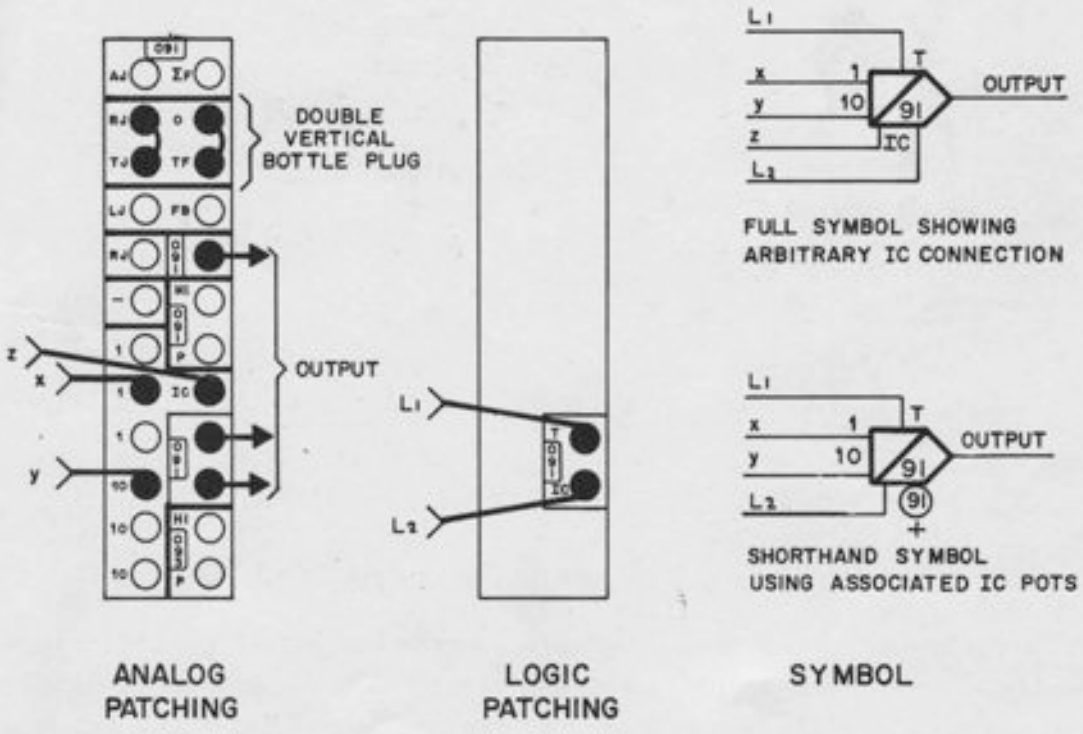


Figure A1.12. Conventional Track/Store Unit

The "TIC" (Track/Store IC) logic input on each track/store unit is normally connected to a "Track/Store IC bus" which is terminated in the MASTER MODE CONTROL AND TIMER tray. (See Paragraph 20.3.7.) This feature permits control of many track/store IC's from a single source. Patching into the "TIC" input on an individual track/store unit frees that particular input from the main track/store IC bus.

1.5.2 Track/Store Unit - Pot Feedback

Figure A1.13 shows a track/store unit with pot-feedback. Note that the double-vertical connection is left intact, and an *additional* connection is made to the ΣF. The symbol shows the abbreviated IC notation. Note that the pot with the same address is used as the IC pot, and that the other pot in the same tray is used as the feedback pot. Of course, any pots could be used, but this assignment of pots allows patching with short leads and bottle-plugs.

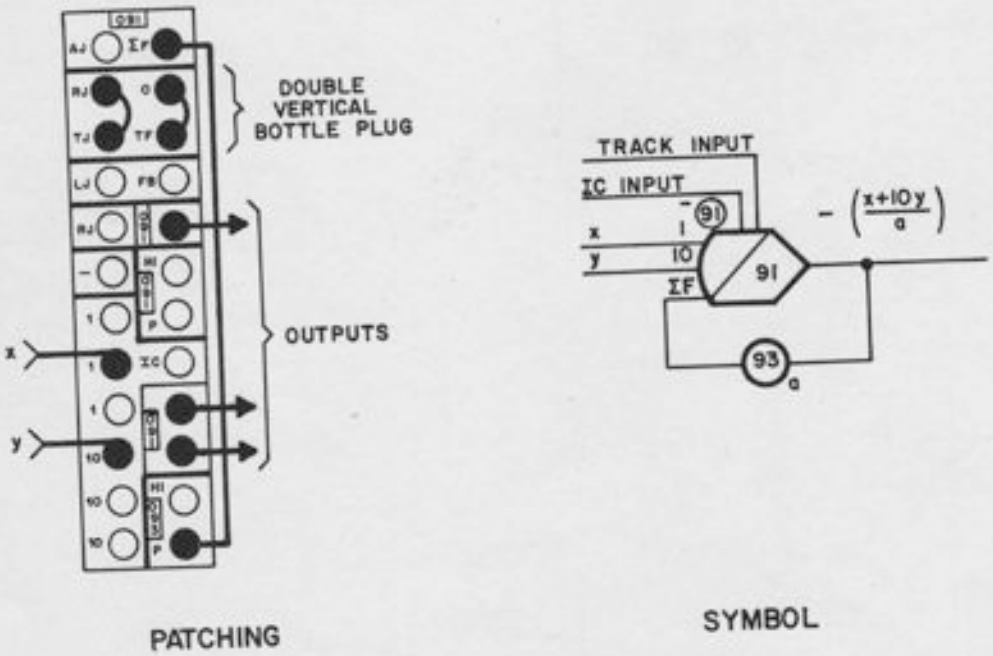


Figure A1.13. Track/Store Unit with Pot Feedback

When the unit is in the *track* mode, it behaves like a regular pot-feedback summer; the output is -(x+10y)/a. The *store* mode and *IC* modes operate in the same manner as with a regular track/store unit. The analog IC input is *not* divided by the setting on the feedback pot. Note that if two logic inputs are drawn, the one *nearer* to the IC pot is assumed to be the logic IC input. This convention eliminates the need for individual labeling of logic inputs. However, if desired, the inputs may be labeled "TIC" and "T".

1.5.3 Track/Store Unit with Arbitrary Feedback

Inserting a pin into the ΣF terminal to a track/store summer disconnects the feedback resistor. The unit may then be used as a high-gain amplifier with arbitrary feedback connection. Any input and feedback networks could be used - linear or non-linear. Such an amplifier may be used, for example, as the output amplifier for a sin/cos DFG or a log/exponential DFG. It will produce the usual output (sine, cosine, log, exponential, etc.) when in the *track* mode, and will hold this value when switched to the *store* mode. Appropriate symbols and a patching diagram are given in Figure A1.14.

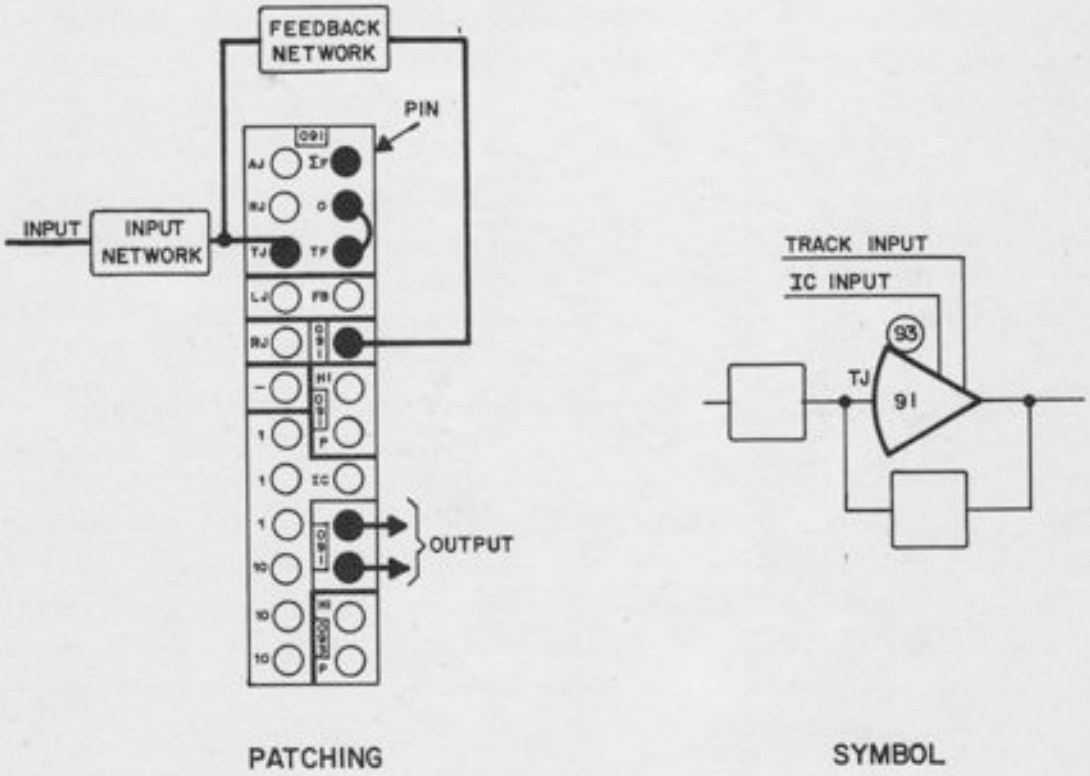


Figure A1.14. Track/Store Unit with Arbitrary Feedback

1.5.4 Using the Combination Amplifier as a Track/Store Unit

For problems requiring more track/store units than the number available in the computer, a combination amplifier may be used as a track/store unit. A patching diagram and programmer's symbol are given in Figure A1.15. The patched logic input nearer to the analog IC input on the diagram is the IC logic input; the other input (the pin) is the OP input.

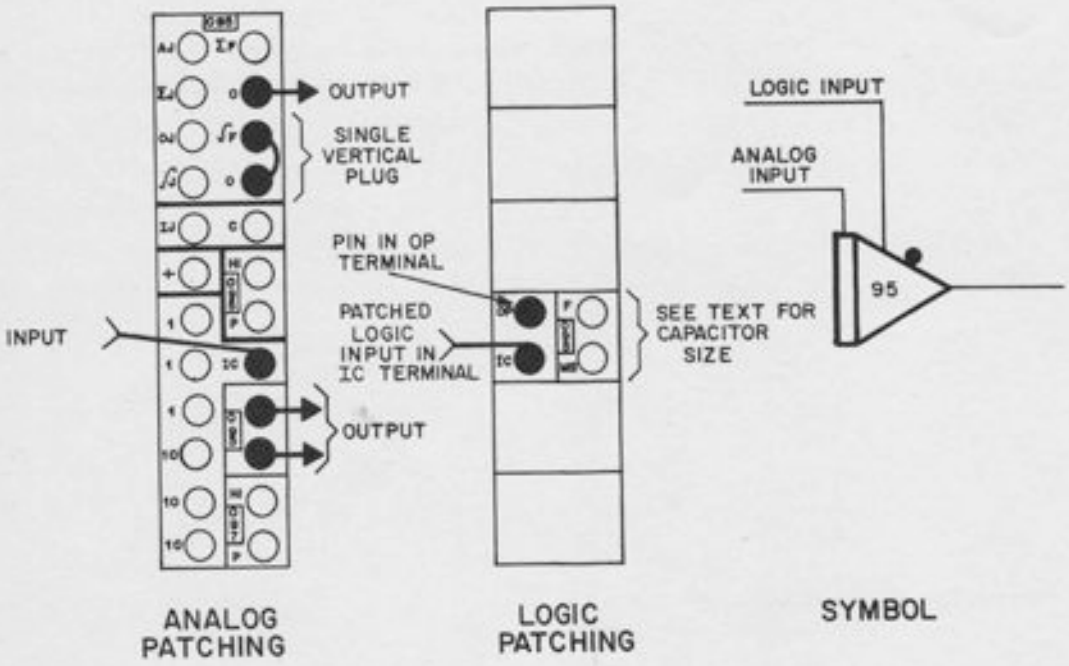


Figure A1.15. Using the Combination Amplifier as a Track/Store Unit

When the logic input is high, the integrator is in the *IC* mode, and follows the patched IC analog input. When the logic input becomes low, the unit switches to the *operate* mode. Since there are no rate inputs, the integrator output remains constant. Hence, the logic input performs the function of the TRACK input on a track/store unit. The integrator *IC* mode corresponds to the *track* mode of a track/store unit; the *operate* mode of the integrator corresponds to the *store* mode of a track/store unit.

As shown in Figure A1.15, the circuit is a single-input track/store unit. However, multiple inputs may be obtained by patching ΣJ to IJ; this allows the entire network of seven resistors (including the feedback resistor) to be used as inputs.

The capacitor value should be chosen to provide the best compromise between minimum lag when tracking (which requires a small capacitor) and minimum drift when storing (which requires a large capacitor). As a general rule, the capacitor selection should be the same as that of the integrator(s) in the loop generating the signal to be tracked. Note that this compromise is not necessary for a track/store summer; the track/store summer contains a switching network that allows it to track with a small capacitor and store with a large one.

1.6 HIGH-GAIN AMPLIFIERS

For applications requiring high-gain amplifiers with externally-patched feedback, the Junction Inverter may be used. Inserting a pin into the "HG" terminal removes the feedback resistor and makes the unit a high-gain amplifier. It is also possible to use a summer or combination amplifier as a high-gain amplifier by removing the bottle plug and patching directly into the Amplifier Junction. However, it is usually preferable to save these amplifiers for multi-input summation and integration. Figures A1.16 through A1.19 give the patching and programmer's symbols.

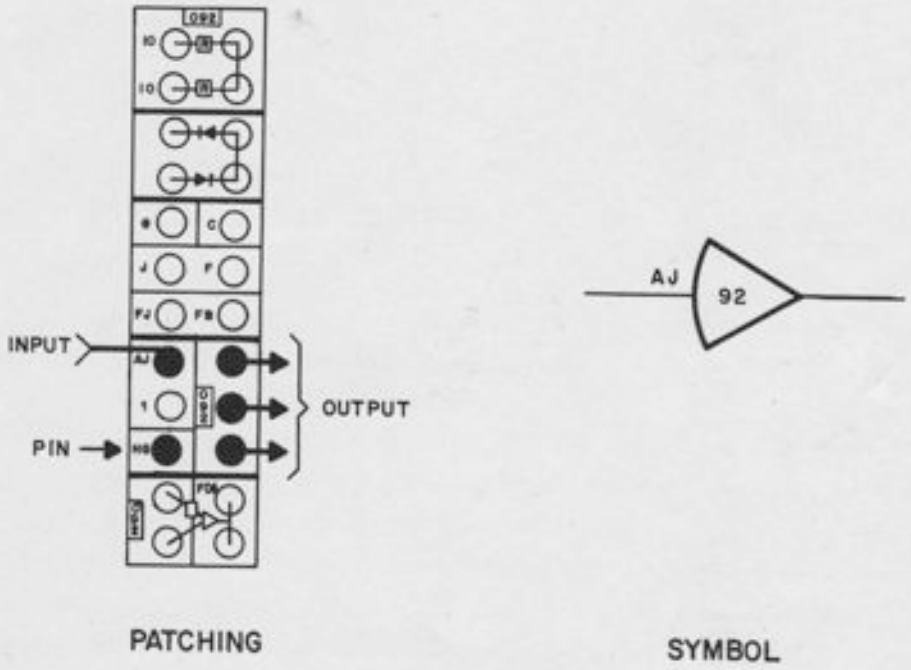


Figure A1.16. Using the Junction Inverter as a High-Gain Amplifier

1.7 ZERO LIMITING

All summers whose address ends in -6, and all Junction Inverters in log/exponential DFG trays contain limit networks which allow the amplifier output to be limited to positive values only or to negative values only. The limit is a very "hard" limit, with a sharp corner and a slope of essentially zero in the limited region. The theory of this limit network is explained in Paragraph 7.2.3, and some typical applications are given in Paragraph 7.2.2.

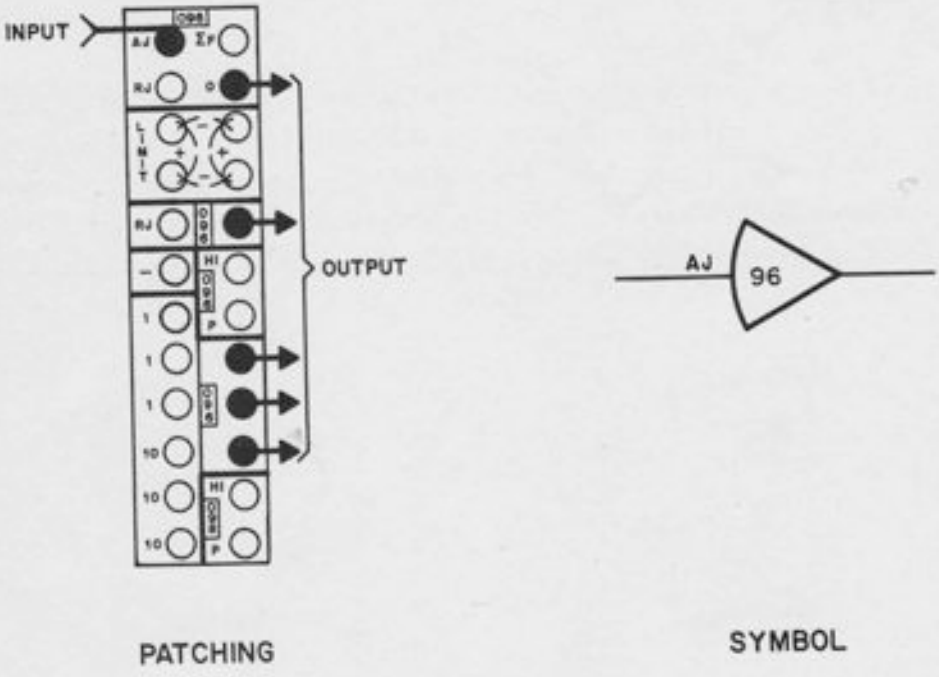


Figure A1.17. Using the Limit Summer as a High-Gain Amplifier

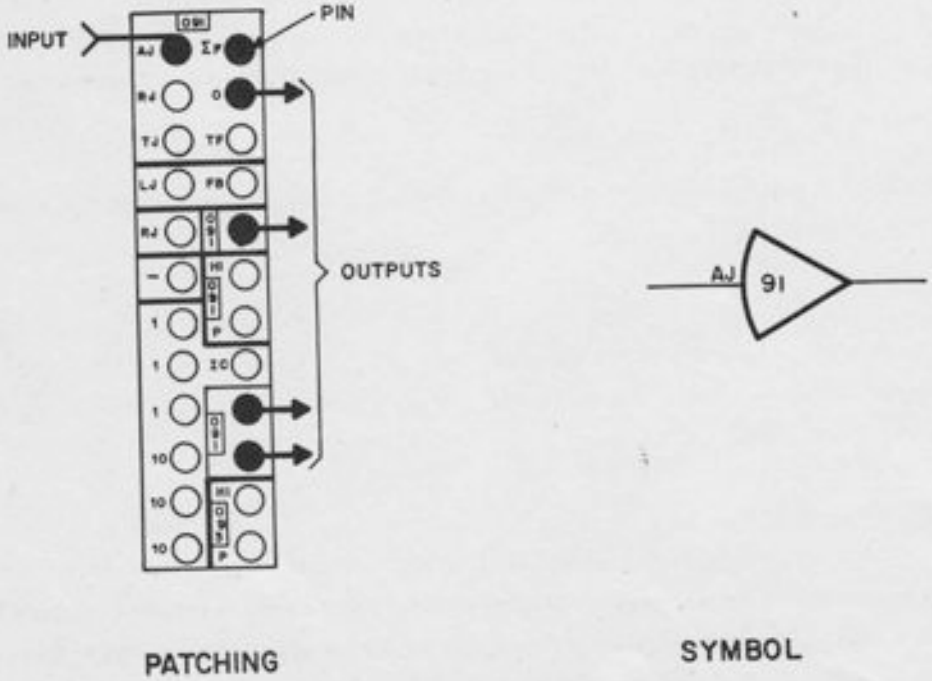


Figure A1.18. Using the Track/Store Summer as a High-Gain Amplifier

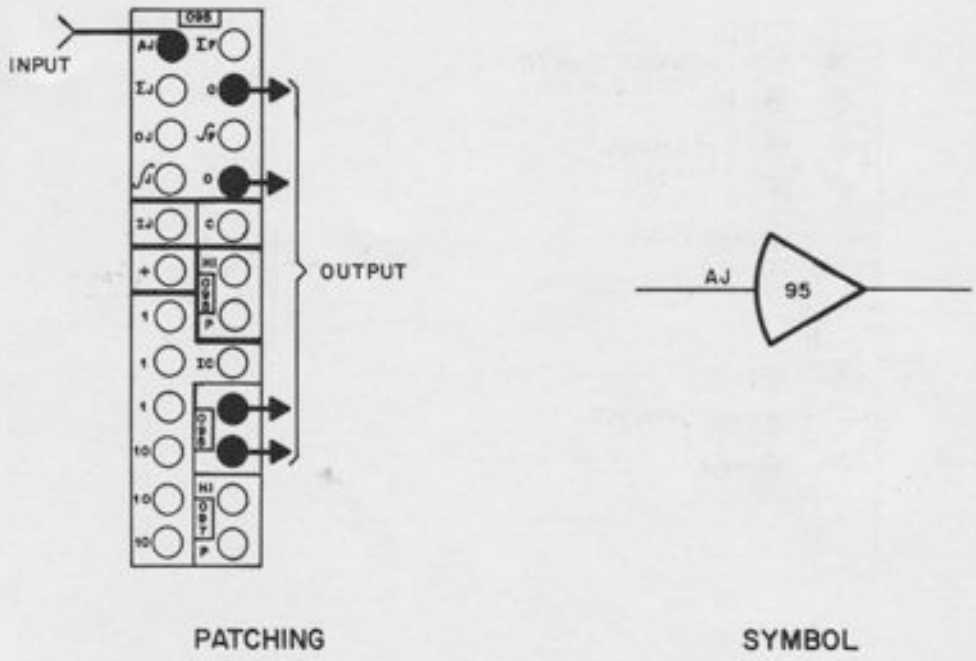


Figure A1.19. Using the Combination Amplifier as a High-Gain Amplifier

To limit one of these amplifier outputs to positive values, all that is required is a double vertical plug in the LIMIT patching area; the remaining patching is the same as it would be without the limit (e.g., summer patching, high-gain patching, pot-feedback patching, etc.). A notation "+LIM" is written on the diagram under the amplifier output. Figure A1.20 gives patching and symbols.

Patching horizontally instead of vertically limits the output to negative values; the notation "-LIM" is used on the diagram.

The rule given in Paragraph 7.2.3 should be observed; the feedback should be resistive only, and all loads should be resistive only. The only exception to this rule is the log/exponential DFG, which *may* be used as a feedback element, or as a load on the amplifier output, since it is designed for such use.

1.8 FEEDBACK LIMITERS

Feedback limiters allow the output of an amplifier to be limited to arbitrary positive and negative values. They may be used with any amplifier whose junction appears on the patch panel. A typical patching diagram and symbol are given in Figure A1.21. Note that a multiple connector is necessary for the $\int J$ when patching a limiter to an integrator.

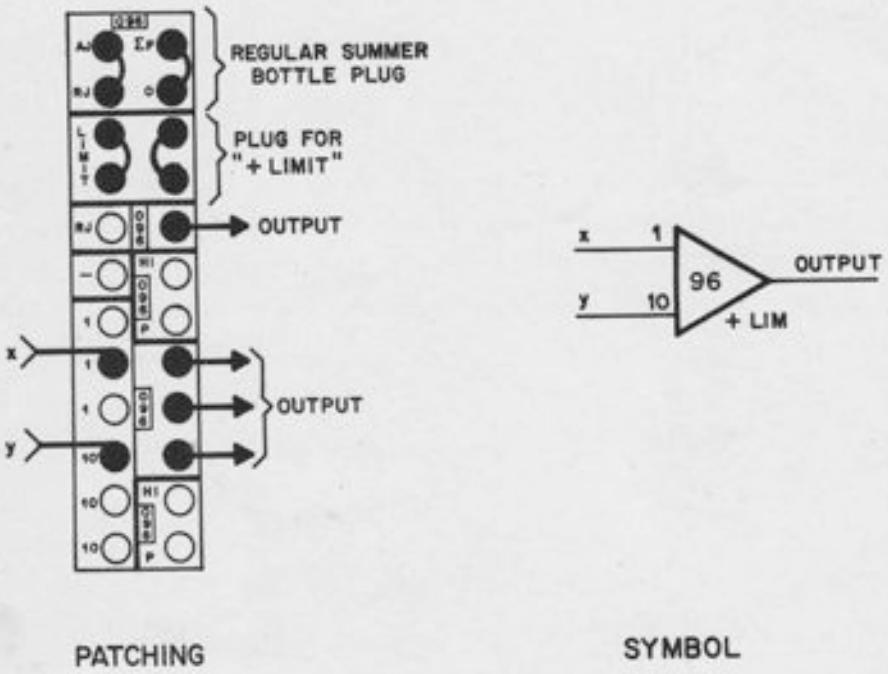


Figure A1.20. Limiting the Limit Summer to Positive Outputs

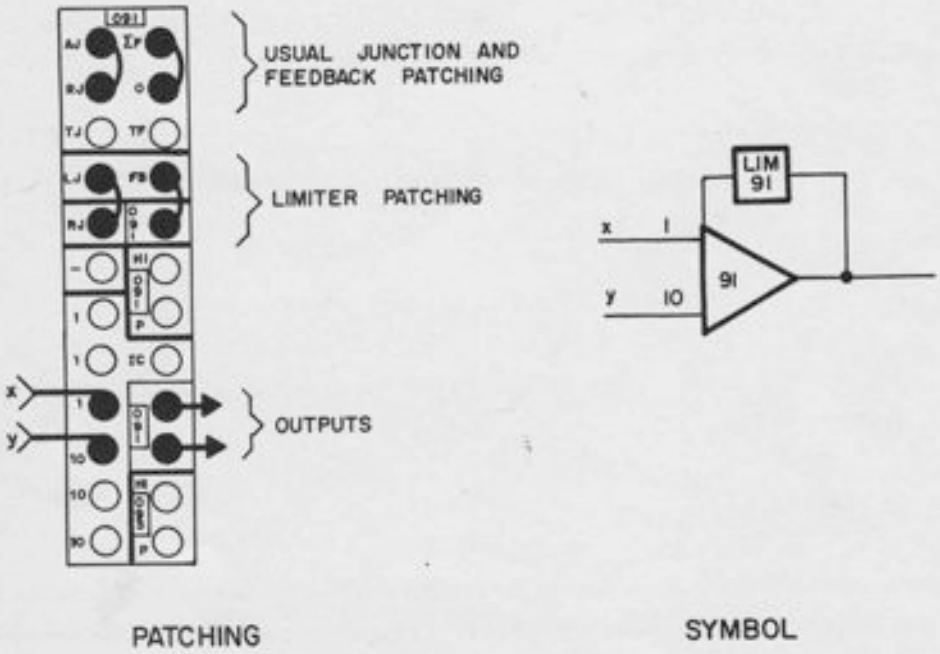


Figure A1.21. Feedback Limiter, Symbol and Patching

1.9 POT APPLICATIONS

The conventional use for a pot is as an attenuator - to multiply by a constant. All 120 servo-set pots and 12 handset pots may be used in this way. In addition, all pots whose address ends in -4 or -9 are three-terminal pots. These pots may be used as conventional attenuators without the necessity of patching the LOW end to ground, since this connection is automatically made with normally-closed patch panel contacts. Typical symbols and patching for two-terminal and three-terminal pots are given in Figures A1.22 and A1.23 give the appropriate patching and programmer's symbols.

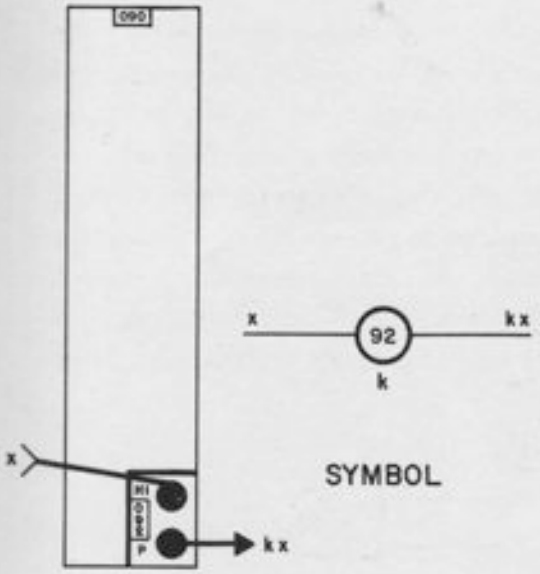


Figure A1.22. Two-Terminal Pot, Typical Symbol and Patching

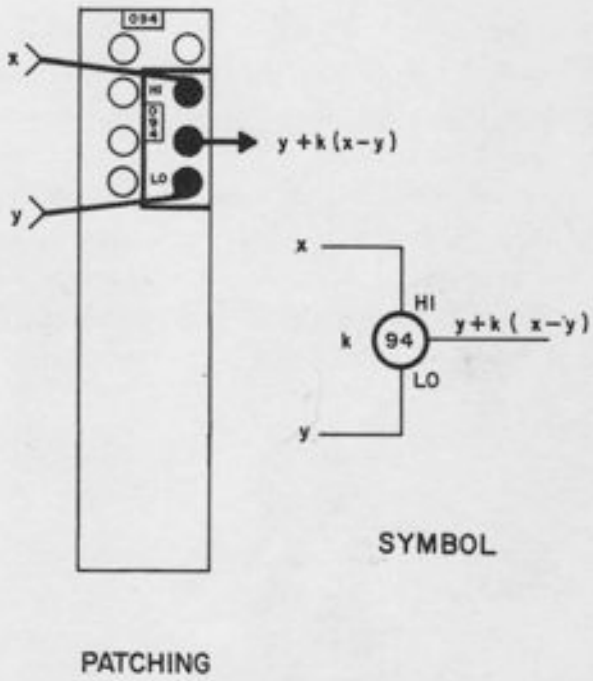


Figure A1.23. Three-Terminal Pot, Typical Symbol and Patching

For some special applications, it is desirable to use a three terminal pot as an adjustable resistor, without the lower end grounded. To free the pot for general-purpose use, it is necessary to patch something (either a pin or a patch cord) into *each* of the end terminals (HI and LO) to break all normally-closed connections.

1.10 MULTIPLICATION

The 680 Quarter-Square Multiplier has been designed to allow the simplest possible programming and patching, without loss of flexibility. The result is a multiplier that may be considered, for most applications, as a three-terminal device (a "black box") which accepts inputs X and Y and produces the output -XY. This result is achieved without the waste of amplifiers or loss of flexibility that would result from building three amplifiers permanently into the unit. This combination of convenience and flexibility depends upon two things; the arrangement of the output amplifier (which is *associated* with the multiplier, but not *committed* to it) and the establishment of a programming and patching convention for the necessary input inverters.

1.10.1 The Output Amplifier

The output amplifier for the multiplier appears in the same tray, and may be connected to the multiplier by a double-vertical plug. Under normal conditions, the multiplier and amplifier may be considered a single unit, with the product appearing at the output terminals of the amplifier. For special applications, such as trigonometric resolution, in which it is necessary to use several multipliers with the same output amplifier, this plug may be removed. Note from Figure A1.24, that the multiplier *without* the output amplifier is represented by a square box; in normal operation, using the associated output amplifier, the square symbol for the multiplier is "merged" with the triangular amplifier symbol to provide a single symbol for the unit as a whole. Note also that *both* the XJ and the YJ should be patched to the AJ of the output amplifier.

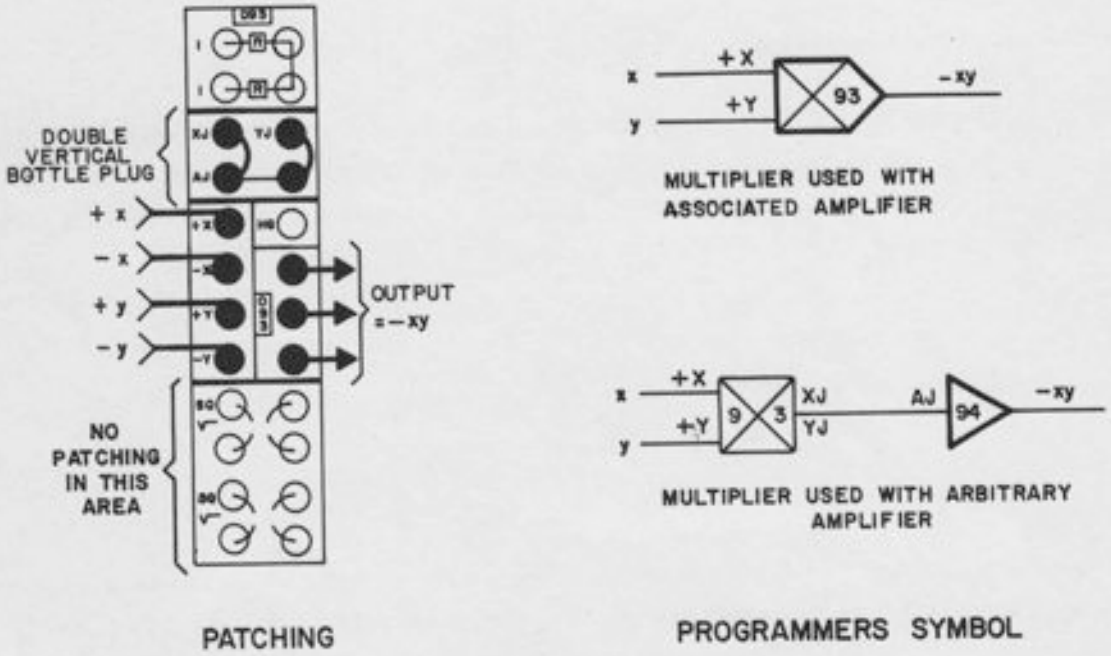


Figure A1.24. Multiplier Symbols and Patching

1.10.2 The Inverters

A quarter-square multiplier must receive both signs of each input, i.e., ±X and ±Y for proper operation. Programming is simplified, and the circuit diagram is made "cleaner" by adopting the convention that, *unless other patching is explicitly indicated,* the -X terminal will be patched to the negative of the +X input, and the -Y terminal to the negative of the +Y terminal. With this convention, it is only necessary to draw *two* inputs, rather than all four. Figure A1.24 shows the programmer's symbol and the actual patched connections for multiplication. Each input drawn represents *two* patching connections. If the input variable Y were drawn connected to the -Y terminal, it would automatically be assumed that the opposite polarity was to be connected to the +Y terminal. The output then would be +XY, rather than -XY.

Note that this convention does not eliminate the necessity for *actually patching* all four inputs, but it simplifies the circuit diagram, and allows the programmer to think essentially in terms of "black-box" multipliers with two inputs and one output. Of course, the programmer must also remember to generate both signs of the input variables; this is usually done with a Junction Inverter or the output amplifier of an unused DFG. It is recommended that this inverter be drawn on the circuit diagram *as close as possible to the amplifier which it inverts,* so that it becomes immediately evident on inspection of the diagram that both signs of this variable are available.

1.10.3 Multiplication with Pot Feedback

The output of a quarter-square multiplier may be multiplied or divided by a constant factor by the use of pot feedback. The amplifier output should be patched to the pot input, and the pot output patched to the "HG" terminal. The appropriate programmer's symbol is given in Figure A1.25; the patching should be obvious from this diagram. Any pot may be used.

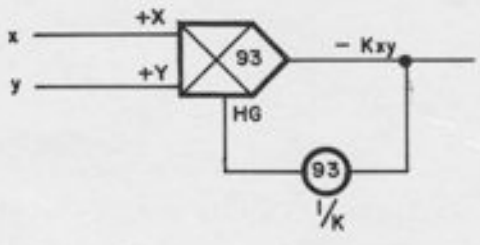


Figure A1.25. Multiplication with Pot Feedback

1.11 DIVISION

Division is obtained by using the multiplier in the feedback path of the amplifier (Figure A1.26). The double-vertical bottle plug used for multiplication is used in the same way for division. Since the multiplier is in the feedback path of the amplifier, and since the multiplier requires both signs, the output must be inverted, using an externally-patched amplifier. The amplifier in the tray to the right of the multiplier is a convenient one to use, but of course, any inverter on the patch panel may be used. Note that both signs of the quotient are produced.

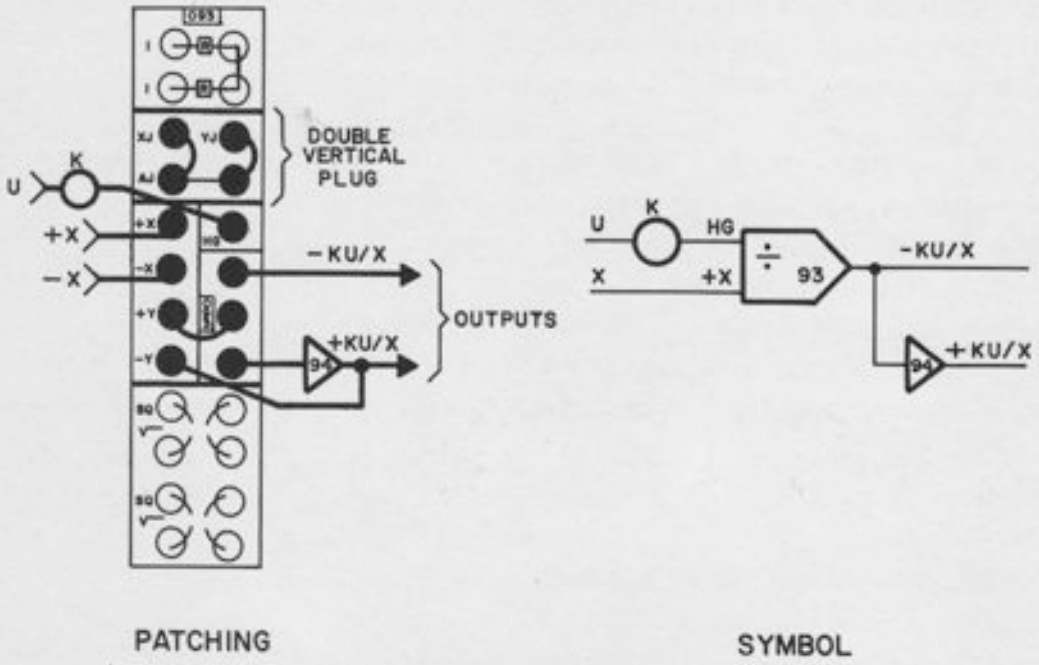


Figure A1.26. Symbol and Patching for Division

The denominator X must be positive, and greater than the numerator in magnitude. Proper scaling of the quotient is obtained by estimating the maximum value of the quotient, and using a pot to attenuate the numerator if necessary. The numerator may be either positive or negative.

1.12 SQUARING

Generating the square of an input variable may be accomplished by using one of the DFG's built into a quarter-square multiplier. Each multiplier contains two such DFG's which are normally connected together for multiplication and division. If the eight-terminal control area at the bottom of the tray is covered by two double-vertical plugs, the two DFG's are freed for independent use. To use one of these DFG's, its output junction (XJ or YJ) should be patched to

the AJ of an amplifier with 10K feedback, such as the associated output amplifier or one of the Junction Inverters. One of the DFG's produces a negative output ($-X^2$); the other produces a positive output ($+Y^2$).

These DFG's may be used with the associated output amplifier, or with any amplifier. For programming convenience, the following conventions are recommended for use on circuit diagrams:

1. If a DFG network is used with its associated output amplifier, the DFG and amplifier may be considered as a single unit and drawn accordingly. If it is used with any other amplifier, the DFG and amplifier should be drawn as separate components. This is the same convention that was suggested in Paragraph 1.10 for the multiplier. Note that the use of a *multiplier* with any amplifier other than the associated amplifier is comparatively rare, since there is an output amplifier for every multiplier; however, when the multiplier is separated into two squaring units, there is only one output amplifier associated with both DFG's. Hence, the use of an amplifier other than the associated one is more common with squaring than with multiplication.

2. Both signs of the inputs are required, except as noted below in Paragraph 3. It is recommended that only *one* input be drawn. This is the same convention that was suggested in Paragraph 1.10 for the multiplier; if a variable is patched to the +X terminal, the negative of that variable should be patched to the -X terminal. Hence, *one* input drawn on the diagram corresponds to *two* patched connections.

   These conventions are illustrated in Figures A1.27 and A1.28 for DFG 1. DFG 2 may be used similarly, either with the associated amplifier or another amplifier. In any case, the amplifier output is $+Y^2$. Note that DFG 1 and DFG 2 produce outputs of opposite polarities. It is *not* possible to change the polarity of the output of either DFG by interchanging the ± inputs.

3. Variables of One Sign Only. The circuits in Figures A1.27 and A1.28 work for both signs of x and y; i.e., the output is correct for $-1 \leq x \leq +1$ and $-1 \leq y \leq +1$. However, if an input does not change sign, it is possible to eliminate an inverter in these circuits, as follows:

   1. If x is always *positive*, then the -x input may be omitted; the -X terminal should be grounded instead.
   2. If y is always *negative*, then the -y input may be omitted; the -Y terminal should be grounded instead.

In both cases, the output will be correct as long as the inputs have the appropriate polarity. For inputs of the wrong polarity, the output will be zero.

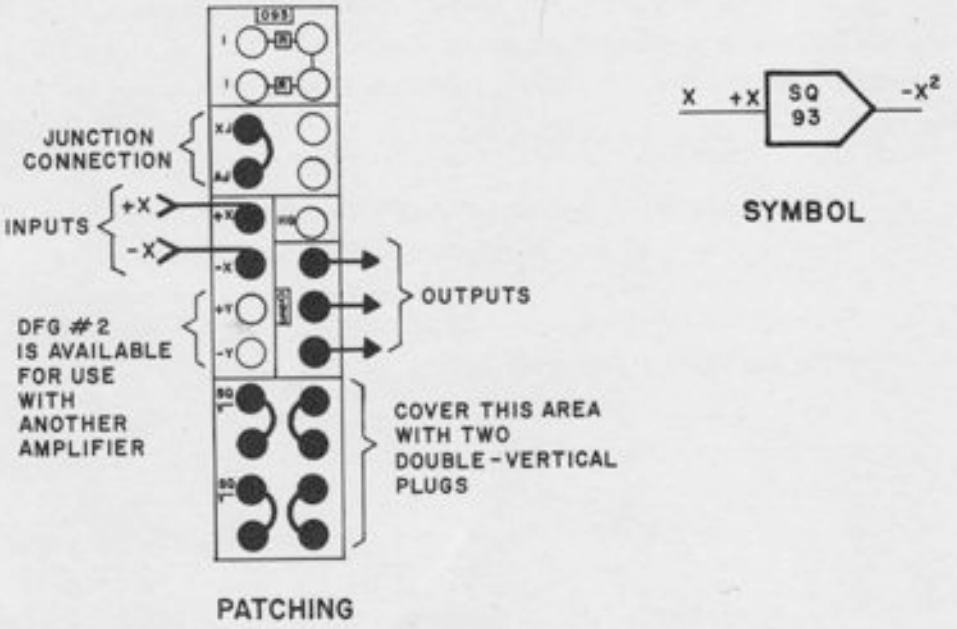


Figure A1.27. Squaring with DFG 1 and Associated Amplifier

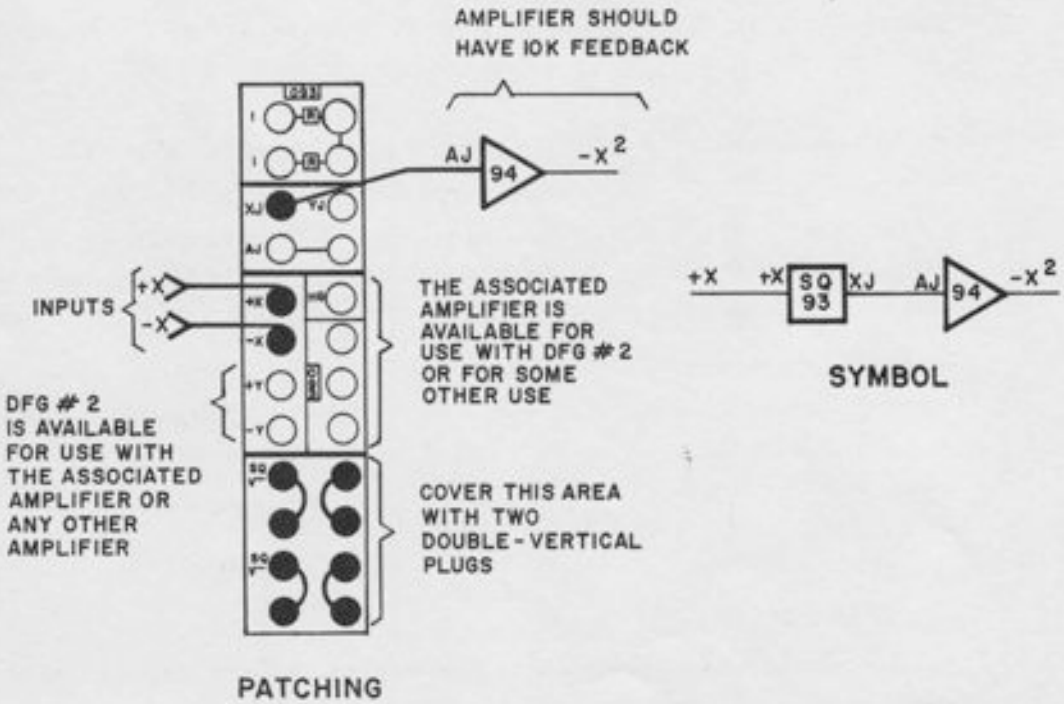


Figure A1.28. Squaring with DFG 1 and Another Amplifier

1.13 SQUARE ROOTS

Either or both of the squaring DFG's may be used to generate the inverse function - the square root. The inverse function is obtained by using the DFG in the feedback path of the amplifier. Hence, the patching is as follows (Figure A1-29):

1. Patch the DFG junction (XJ or YJ) to the AJ of the amplifier.
2. Patch the amplifier output to the +DFG input (+X or +Y).
3. Ground the -DFG input (-X or -Y).
4. Patch the input variable (whose square root is to be generated) into the HG terminal of the amplifier. This makes the 10K feedback resistor serve as an input resistor.

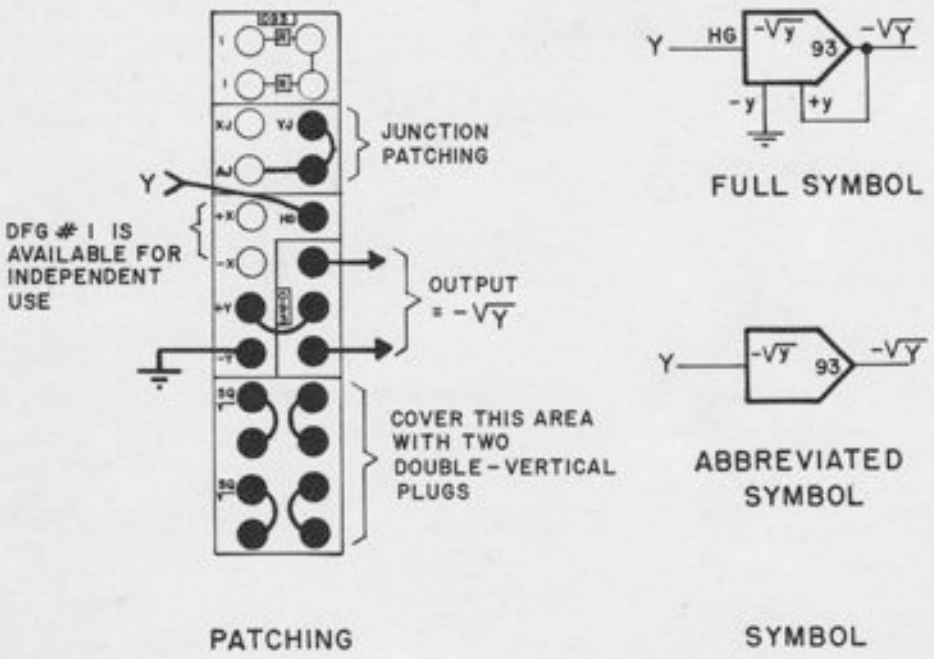


Figure A1.29. Square Root Circuit, DFG 2

When DFG 1 is used in this manner, the input must be *negative*. If the input is x, the output is $+\sqrt{|x|}$. For DFG 2, the input must be *positive*. The input y will produce the output $\sqrt{y}$.

The square circuit for DFG 2 is shown in Figure A1.29. Note that, since the associated amplifier is used, the amplifier and the DFG are drawn as a single unit. A further abbreviation of the symbol is also suggested, which omits drawing the feedback connection to -Y. If this symbol is used, these connections are understood to be implicit in the "$\sqrt{y}$" symbol.

The circuit for DFG 1 is similar, except for the reversal of input and output polarities as noted above. When one of the DFG's is used for a square root, the other one is available for either square or square root use.

1.14 GENERATING -x|x|.

In many applications, (for example, viscous damping) it is desired to generate an output voltage whose magnitude is proportional to the square of the input, but whose sign changes as the input passes through zero. Such a function may be described mathematically by $f(x) = x \cdot |x|$. Although this quantity could be generated by a standard absolute value circuit (see the applications of the limit summer) and a multiplier, it is more accurate and more economical to use the two squaring cards in the quarter-square multiplier to generate the positive and negative parts of the function. Note that both DFG's are required. See Figure A1.30 for the patching and symbols.

1.15 GENERATING -(sign x) · $\sqrt{|x|}$

The inverse of $x|x|$ is (sign x)$\sqrt{|x|}$. This function is occasionally useful in fluid-flow problems. Patching and symbol are given in Figure A1.31.

1.16 THE LOG FUNCTION

Each log/exponential DFG tray contains two DFG networks; a "plus" network and a "minus" network. Each is intended for use with an amplifier with a 10K feedback resistor. A Junction Inverter with 10K feedback is also located in the tray. The "plus" and "minus" DFG's behave identically except for polarity of inputs and outputs.

To generate the log function of a variable x, the input x is patched to the appropriate input terminal (+IN or -IN) and the FJ (Function Junction) immediately below the input is patched to the AJ of the output amplifier.

This appendix contains only the patching instructions and programmer's symbols for the *simplest* log and exponential circuits. More detailed programming and scaling information is given in Appendix 4.

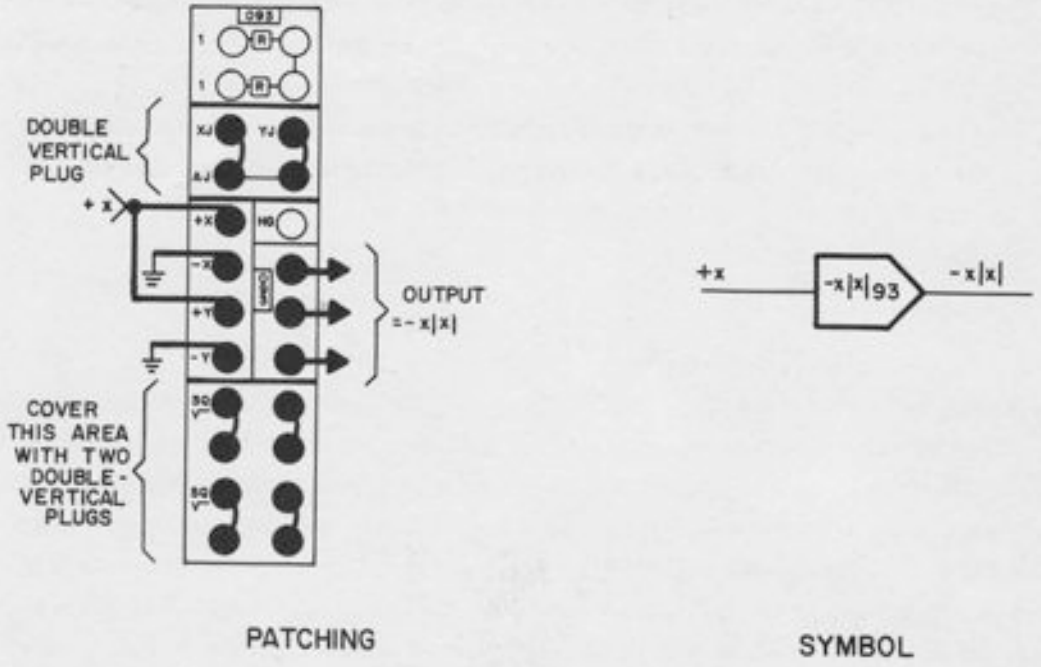


Figure A1.30. Generating -x|x|

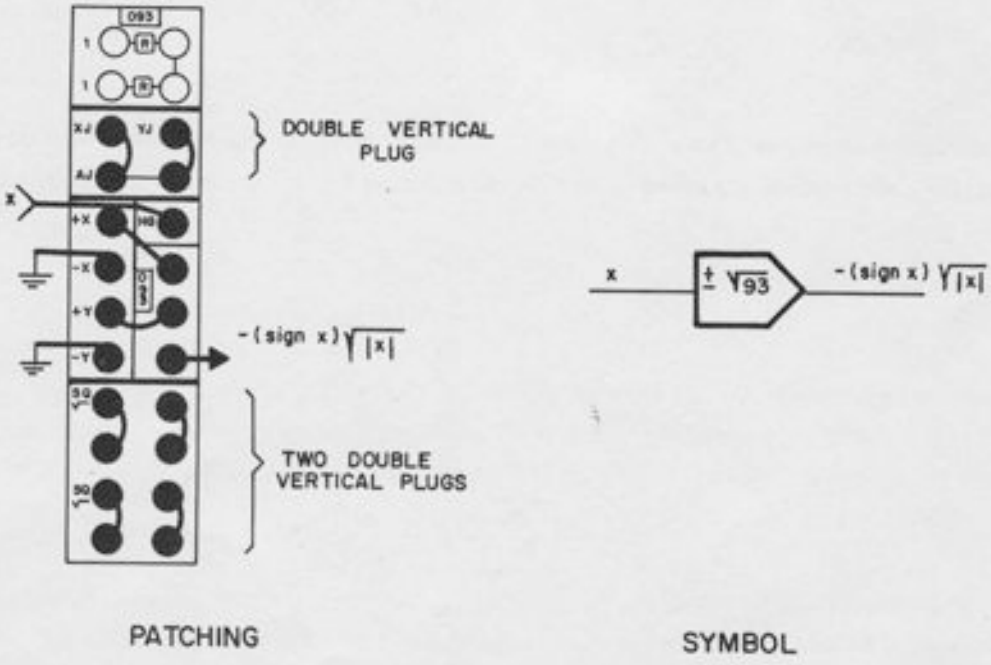


Figure A1.31. Generating -(sign x)√|x|

1.16.1 The "Plus" Network

When the "plus" network is used, the input x must be *positive*, and the amplifier output is -0.1 $\log_e x$. Appropriate programming symbols are given in Figure A1.32. Note that the square symbol for the DFG network and the triangular amplifier symbol may be merged into one symbol if the DFG network is used with the associated amplifier. If it is used with another amplifier, the network and amplifier should be drawn separately. In any case, an amplifier with 10K feedback should be used, such as a Junction Inverter or the output amplifier of an unused quarter-square multiplier.

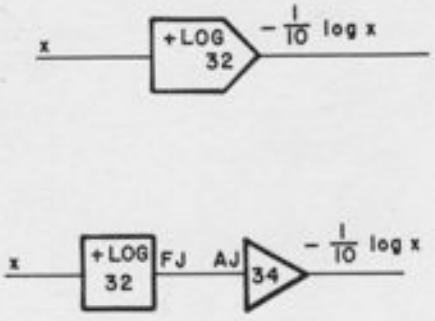


Figure A1.32. Logarithm, Using the +Log Network

1.16.2 The "Minus" Network

If the "minus" network is used, the input x must be negative, and the amplifier output is +0.1 $\log_e |x|$. Programmer's symbols are given in Figure A1.33, the same comments apply as for the "plus" network.

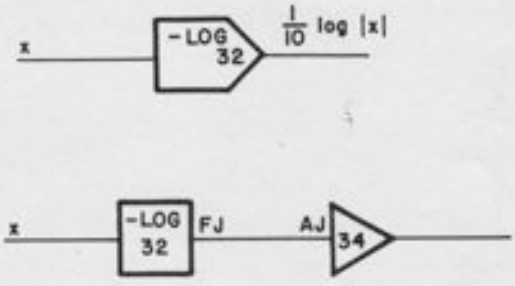


Figure A1.33. Logarithm, Using the -Log Network

1.17 THE EXPONENTIAL FUNCTION

The exponential function is the inverse of the logarithm, and hence may be obtained by using a log DFG in the feedback of an amplifier. The FJ of the DFG network is patched to the AJ of the amplifier, just as for log generation, but the input is patched to the "HG" terminal of the amplifier, which breaks the feedback resistor connection. The output of the amplifier is patched to the +IN or -IN terminal thus putting the DFG itself in the amplifier feedback path. More detail on programming and scaling the exponential function is given in Appendix 5.

1.17.1 The "Plus" DFG

Figure A1.34 shows programmer's symbols for the exponential using the "plus" DFG. For DFG and amplifier in different trays, the symbol shows explicit patching connections; for a DFG and amplifier in the same tray, an abbreviated symbol is shown. Note that in the abbreviated case, the input is not explicitly labeled "HG"; the "+EXP" notation is understood to imply the actual patching.

Figure A1.34. Exponential, Using the +Network

1.17.2 The "Minus" DFG

The "minus" DFG may also be used for exponential generation. The same comments about notation apply as for the "plus" DFG.

1.18 THE SINE FUNCTION

The Function -sin θ may be obtained with the sin/cos DFG and one or two amplifiers. If $|\theta| \leq 90°$, the function is monotonic decreasing, and a single amplifier is required. If θ ranges from -180° to +180°, then two amplifiers are required; an output amplifier, and a "shaping amplifier". Input scaling (in units) is (θ/200) , so that the maximum allowable value of θ (±180°) corresponds to ±0.9000 unit (±9 volts).

The DFG uses non-linear feedback; hence, the regular 10K feedback resistor must be removed by inserting a pin into the "HG" terminal. This must be done for both the shaping amplifier and the output amplifier.

In assigning components, it is suggested that the associated amplifier (in the same tray) be used as the output amplifier, and some other amplifier be chosen for the shaping amplifier. Both explicit programming symbols and abbreviated symbols are given in Figure A1.35. The explicit symbols show all patching connections between the DFG and the amplifiers. The abbreviated symbols show only input and output connections; the notation "-sin" in the symbol implies the necessary "setup" connections.

Note in Figure A1.35, that *both* the number of the shaping amplifier and the number of the output amplifier are written on the symbol. By convention, the number of the output amplifier is written closer to the output side of the symbol; if the abbreviated notation is used, the output amplifier should be the one in the same tray as the DFG.

In the sine and cosine circuits, the load on the "θ" input is linear (resistive). Hence, it is permissible for the θ input to come either from an amplifier or from a pot.

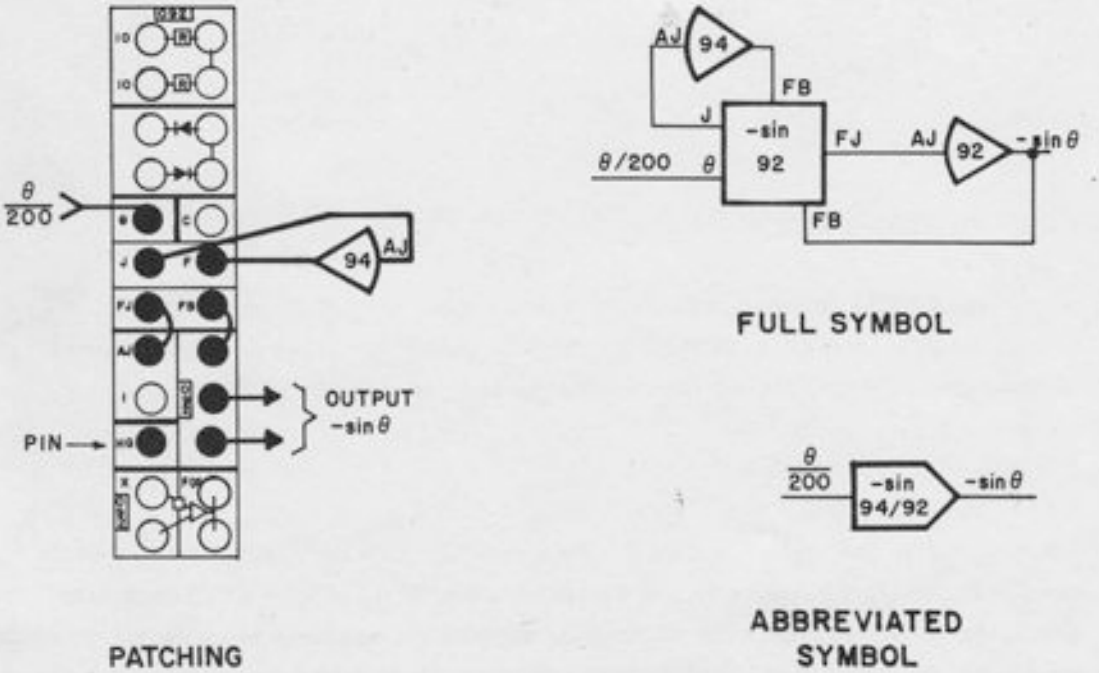


Figure A1.35. Symbol and Patching for -Sin θ

1.19 THE COSINE FUNCTION

The cosine function, like the sine function, may be generated over a restricted range with a single amplifier, or over a full revolution (±180°) with two amplifiers. The same conventions are recommended as with the sine function: the output amplifier should be the associated amplifier in the same tray, and the number of the output amplifier should be written closer to the output side of the symbol.

The "C" (Control) terminal should be connected to -Reference (to generate +cos θ). The "Control" terminal adds a constant bias to the input to "shift" the sine function 90° to the left or the right, producing the cosine function. Patching "C" to -Reference produces +cos θ; patching "C" to +Reference produces -cos θ. Figure A1-36 illustrates the programmer's symbol for a sine/cosine generator patched to produce an output of +cos θ.

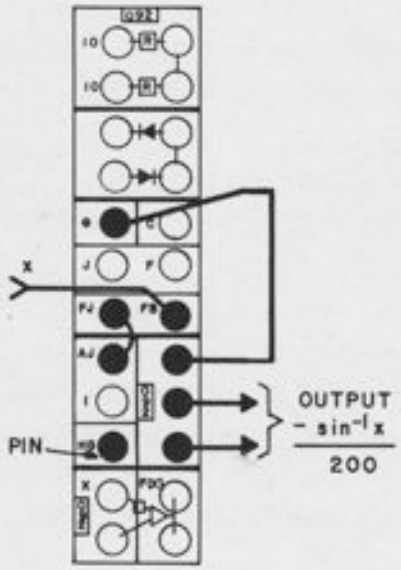
Figure A1.36. Programmer's Symbol for +Cos θ

1.20 INVERSE TRIG FUNCTIONS

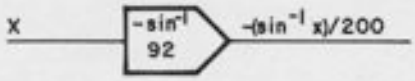
Interchanging input and feedback connections on a sin/cos DFG produces the inverse trigonometric function. Since the functions involved are monotonic over the region of interest, only one amplifier is needed.

1.20.1 Arcsine Function

Patching and an abbreviated symbol for the arcsine function are given in Figure A1.37. The input x may range from -1 to +1. The output is $-\left[(\sin^{-1}x)/200\right]$, which ranges from +0.45 unit to -0.45 unit. The output scaling would be better if the circuit were modified to generate the output $\left[(-\sin^{-1}x)/100\right]$. This scaling may be obtained with pot feedback, as shown in Figure A1.38. The pot input is patched to the amplifier output and the pot output is patched to the "9" input.



PATCHING



SYMBOL
(ABBREVIATED)

Figure A1.37. Symbol and Patching for Inverse Sine Function

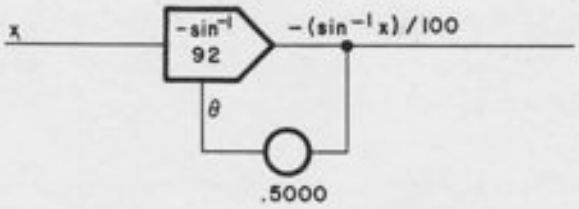


Figure A1.38. Inverse Sine Function with Pot Feedback

1.20.2 Arc Cosine Function

The inverse cosine input may be obtained by patching the "C" terminal to -Reference in Figure A1.38. The output will be $\left[(\cos^{-1} x)/200\right]$, which ranges from -0.9000 unit when x = 1, to zero when x = +1. Since the output reaches a maximum value of 90% of reference voltage, pot feedback is not recommended. The programmer's symbol is the same as in Figure A1.38, except that the notation "COS^{-1}" is used inside the symbol.

1.21 ARBITRARY FUNCTIONS

Arbitrary functions (given in graphical or tabular form) may be set on variable DFG's. A programmer's symbol for a variable DFG is given in Figure A1-39. The use of the letter "F"

rather than a specific function name such as "LOG" or "EXP" indicates that this is an arbitrary function, rather than an analytic function using a fixed DFG. As pointed out in Chapter 10, a graph of the function should be made at the time of setup, and should become part of the problem documentation.

The note in Paragraph 10.4.3 about combined summation and function generation should be observed.

Figure A1.39. Arbitrary Function Generation

1.22 UNCOMMITTED RESISTORS AND BORROWED NETWORKS

Whenever a summer or integrator requires more than the six or seven inputs associated with the amplifier, additional inputs must be patched. (Note than an integrator has effectively *seven* inputs, since the "ΣF" terminal may also be used as an input.) These inputs should be patched to the same terminal as the regular input resistor network (OJ for an integrator, AJ for a summer, TJ for a track/store unit, etc.). Summing amplifiers have the RJ terminated twice, so that an additional network may be patched in without disturbing the regular bottle-plug patching. This is not true for integrators. To add extra inputs to an integrator requires a multiple connection.

Additional input resistors may either be "borrowed" from another amplifier, or one of the "uncommitted networks" in the DFG trays or multiplier trays may be used. In any case, it is recommended that the network be identified on the diagram by the number of the tray in which it appears. This not only facilitates patching, but aids in problems de-bugging, since it is easier to trace a patchcord to its specific patched connection. Figure A1.40 shows suggested symbols for borrowed networks.

NOTE

When "borrowing" the network of a track/store summer for use with some other amplifier, it is necessary to patch something into the ΣF terminal to break the normally-closed connection. Either use the ΣF as a 100K input resistor or insert a pin in this terminal. This requirement does not apply to limit summers or combination amplifiers, which do not use normally-closed terminals for feedback connections.

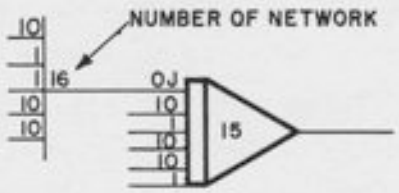


Figure A1.40. "Borrowed" Resistor Network

1.23 THE A/D COMPARATOR

A programmer's symbol for the A/D comparator appears in Figure A1.41. Three inputs are provided; however, the programmer does not have to ground unused inputs, except as noted in Paragraph 13.2.3.1. The "LATCH" input need not be drawn unless it is used. It is normally low if unpatched, and hence, will not effect the behavior of the comparator.

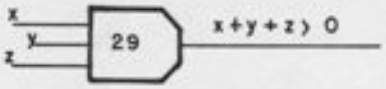


Figure A1.41. Programmer's Symbol, Electronic Comparator

It is often useful to label the output of a comparator with an expression indicating the conditions under which the output is high, such as "x + y > 0", or "x > y", or some other short statement or phrase.

The state of each comparator is indicated by a light on the logic readout panel. See Paragraph 2.5.2.

1.24 ELECTRONIC SWITCHING

Electronic switching may be performed with one of the D/A switches in the interface tray, or with a combination amplifier. The D/A switch is more economical and convenient for turning a single signal off or on. The combination amplifier has the flexibility of allowing many inputs to the same amplifier to be switched simultaneously.

1.24.1 The D/A Switch

The D/A switch is a "switchable input resistor", which must be patched to a virtual ground (AJ, OJ, LJ, TJ, etc.). It may be used to turn a single input off and on for any of the 120 amplifiers whose summing junction appears on the patch panel. For track/store summers and limit summers, the additional connection may be made without disturbing the regular bottle-plug patching, since the RJ (the junction of the regular input resistor network) is duplicated on the patch panel.

For combination amplifiers, the summing junction is not duplicated, so that a multiple connector will generally be necessary to connect both the regular resistor network and the D/A switch. Of course, if the D/A switch is the *only* input to the integrator, the D/A switch output may be simply patched to the OJ and no multiple connector is needed.

Figure A1.42 shows programmer's symbols for the more common D/A switch connections. Note that the D/A switch is a 10K resistor, which gives an effective gain of ten when used with a summer or integrator, and an effective gain of one when used with a junction inverter.

1.24.2 The Combination Amplifier

The combination amplifier is useful in cases where many inputs to one amplifier must be switched on or off by the same logic signal. If D/A switches were used, one switch would be required for each input.

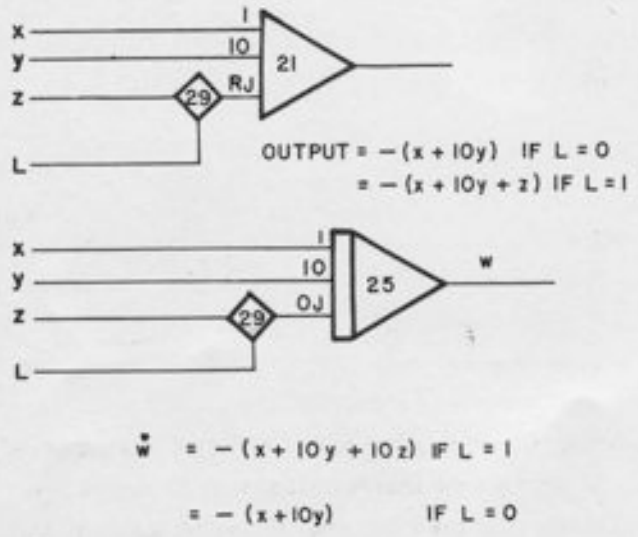


Figure A1.42. Programmer's Symbol for D/A Switch

The use of the combination amplifier for switching depends upon the fact that each such amplifier has two electronic switches for mode control. The patching, which is given in Figure A1.43, is similar to the patching for an integrator (but note the use of three vertical plugs in the control area, and the pin in the "C" terminal to disconnect the feedback capacitor). With this capacitor removed, the "integrator" would have no feedback in the *operate* mode, except for the upper bottle-plug (output to ΣF) which provides a standard 100K feedback resistor. When the "integrator" is in the *operate* mode, all the regular inputs *and* the ΣF feedback resistor are switched on. When the "integrator" is in the *IC* mode, the regular IC input and feedback resistors are switched on.

The "mode control" (which is really *switching* control in this case) is cycled between *IC* and *operate* by the same patching used in Paragraph 1.2.1. Additional inputs may be patched to IJ or OJ as desired.

1.25 RELAY SWITCHING

The D/A relay (also called function relay) is a versatile unit which may be used as a manually-positioned function switch, a D/A relay (positioned by a logic signal) or a set-reset (latching) relay, making use of its internal flip-flop.

1.25.1 Use as Function Switch

If a manually-positioned switch is required, no logic inputs need be patched. The relay is a DPDT switch, which may be positioned by the manual controls, as described in Paragraph 2.5.2. Only the contacts need be drawn on circuit diagrams.

1.25.2 Use as a D/A Relay

A D/A relay is a relay positioned by a logic signal; it is in one position when the logic signal is high, and in another position when the logic signal is low. To use the relay in this mode, it is necessary to patch the logic signal to S+ *and* patch its complement to S-, since the relay contains a flip-flop. A recommended programmer's symbol for this mode of operation is shown in Figure A1.44; in this mode of operation, the logic input is assumed to go to the S+ terminal and its complement to the S- terminal. The relay contacts need not be drawn adjacent to the logic control input on the diagram; they may be drawn wherever convenient. There are two sets of contacts, labeled "A" and "B" on the diagram; this labeling corresponds to the labeling on the analog patch panel.

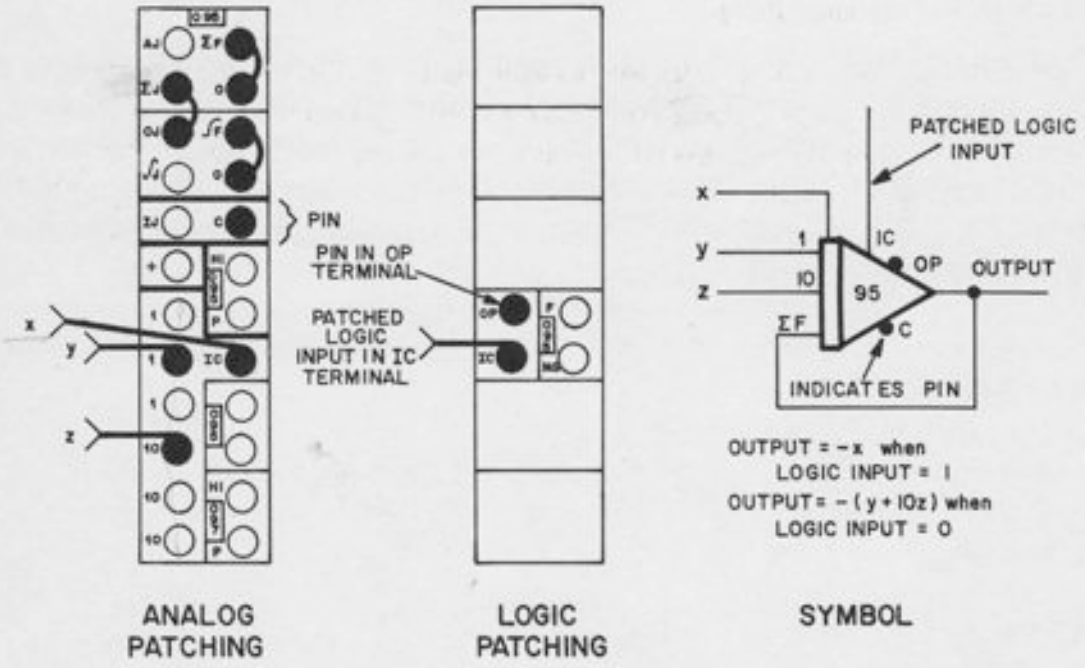


Figure A1.43. Use of the Combination Amplifier as an Electronic Switch

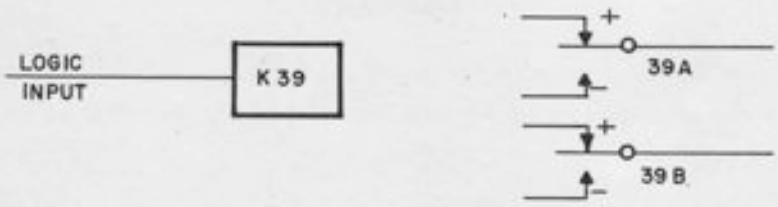


Figure A1.44. Use of the D/A Relay with Complementary Inputs

Figure A1.45. Use of the D/A Relay as a Latching Relay

1.25.3 "Latching" Relay

A set-reset relay, or "latching" relay has two logic inputs, each of which forces the relay to a particular state. When both inputs are simultaneously LOW the relay will remain fixed in its present state. The 680 relay has this feature, which is achieved by means of an internal flip-flop. A recommended programmer's symbol is shown in Figure A1.45. Note the use of a different-shaped symbol than for the simple function relay mode; the oval symbol emphasizes the fact that the unit has a built-in flip-flop.

APPENDIX 2

EQUIPMENT ASSIGNMENT SHEETS

This appendix includes assignment sheets for all major components in the 680. The main purpose of an assignment sheet is to organize the "bookkeeping" involved in the setup and checkout of a problem. In particular, the assignment sheet allows the programmer to keep track of which components have been assigned and which are still available, so that the same component is not assigned twice. Also, the assignment sheets remind the programmer of the structure of the computer - how many components of a given type there are, how they are numbered, etc.

2.1 AMPLIFIER SHEETS (Figures A2.1 and A2.2)

All 120 amplifiers, from A0 to A119 are listed on two sheets in numerical order. Space is provided for indicating the use to which the amplifier is put. The following abbreviations are recommended:

- $\int$ Integrator
- Σ Summer
- PF Pot Feedback
- \- Inverter
- M Multiplier Output
- H High-Gain

Space is provided for indicating the output variable, which should include both sign and scale factor, e.g., -x sinθ/500. A numerical value (calculated for static check purposes) is also provided for. Space is provided for entering a precalculated value for the derivative in the case of combination amplifiers. Note that the area for the derivative is marked off only for combination amplifiers, thus serving as a reminder of which amplifiers may be used as integrators.

2.2 POTENTIOMETER SHEETS (Figures A2.3 and A2.4)

The 120 servo-set pots, numbered 0 - 119 are listed on two sheets in numerical order. Space is included for a parameter expression (such as K/20Mβ) and numerical settings for the static check and the first run. Values for the first run do not need to be entered unless they differ from the static check values.

EAI 680 AMPLIFIER ASSIGNMENT SHEET (A00-A59)

PROBLEM_____ PROJECT# _____

PROGRAMMER_____ CONSOLE_____ DATE_____

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	CHECK VALUE
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				
24				
25				
26				
27				
28				
29				

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	CHECK VALUE
30				
31				
32				
33				
34				
35				
36				
37				
38				
39				
40				
41				
42				
43				
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59				

Figure A2.1. Amplifier Assignment Sheet (A00-A59)

EAI 680 AMPLIFIER ASSIGNMENT SHEET (A60-A119)

PROBLEM _____ PROJECT # _____

PROGRAMMER _____ CONSOLE _____ DATE _____

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	CHECK VALUE
60				
61				
62				
63				
64				
65				
66				
67				
68				
69				
70				
71				
72				
73				
74				
75				
76				
77				
78				
79				
80				
81				
82				
83				
84				
85				
86				
87				
88				
89				

AMP	USE	OUTPUT VARIABLE	CHECK DERIVATIVE	CHECK VALUE
90				
91				
92				
93				
94				
95				
96				
97				
98				
99				
100				
101				
102				
103				
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118				
119				

Figure A2.2. Amplifier Assignment Sheet (A60-A119)

EAI 680 POTENTIOMETER ASSIGNMENT SHEET (P00-P59)

PROBLEM _____ PROJECT # _____

PROGRAMMER _____ CONSOLE _____ DATE _____

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
0			
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
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58			
59			

Figure A2.3. Potentiometer Assignment Sheet (P00-P59)

EAI 680 POTENTIOMETER ASSIGNMENT SHEET (P60-P119)

PROBLEM _____ PROJECT # _____

PROGRAMMER _____ CONSOLE _____ DATE _____

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
60			
61			
62			
63			
64			
65			
66			
67			
68			
69			
70			
71			
72			
73			
74			
75			
76			
77			
78			
79			
80			
81			
82			
83			
84			
85			
86			
87			
88			
89			

POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
90			
91			
92			
93			
94			
95			
96			
97			
98			
99			
100			
101			
102			
103			
104			
105			
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116			
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119			

Figure A2.4. Potentiometer Assignment Sheet (P60-P119)

2.3 NONLINEAR COMPONENTS AND HANDSET POTS (Figure A2.5)

The 12 handset pots and all nonlinear components are included on one sheet.

2.3.1 Handset Pots

These entries are filled in exactly as for servo-set pots.

2.3.2 Limiters

The 12 feedback limiters are listed by number. For each limiter, space is provided for the amplifier to which it is connected, and the limited variable (which is the amplifier output, including sign and scale factor). Space is provided for numerical settings for both static check and actual run conditions.

2.3.3 Variable DFG's

For each variable DFG, there is space to indicate the use (10, 20, INV), the output variable (including sign and scale factor) and a numerical check value. The DFG's in an associated pair, (e.g., 32 and 37) are in the same horizontal row.

2.3.4 Multipliers

For each multiplier, space is provided only for indicating the use, (e.g., M, D, SQ, $\sqrt{\ }$). Output variables and check values are indicated in the entry for the associated amplifier.

2.3.5 Fixed DFG's

For fixed DFG's, space is provided for the type (sin, log) and an indication of the use. Output variables and check values are indicated in the entry for the amplifiers.

2.4 LOGIC SHEET AND INTERFACE SHEET (Figures A2.6 and A2.7)

The space labeled "OUTPUT" or "FUNCTION" for a given component may be filled in with a short verbal or algebraic statement of the conditions under which the output is high. For example "$x > 0$" would be written for a comparator, to indicate that the output is high when $x > 0$. Various mnemonic indications may be used, at the discretion of the programmer. At the very least, a check mark should be made to indicate that the unit is being used, to prevent the component being assigned twice. Systematic checkout of a logic program is easier if most of the principal components are labeled with some indication of their function in the problem.

EAI 680 NONLINEAR COMPONENT ASSIGNMENT SHEET

(MULTIPLIERS, DFG's, LIMITERS, AND HAND SET POTS)

PROBLEM_____ PROJECT #_____

PROGRAMMER_____ CONSOLE_____ DATE_____

HAND POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
2			
4			
7			
9			
12			
14			

HAND POT	PARAMETER EXPRESSION	CHECK SETTING	RUN SETTING
17			
19			
22			
24			
27			
29			

LIMITER	AMP	LIMITED VARIABLE	CHECK SETTINGS +	CHECK SETTINGS −	RUN SETTINGS +	RUN SETTINGS −
1						
11						
21						
31						
41						
51						
61						
71						
81						
91						
101						
111						

VDFG	USE	OUTPUT VARIABLE	CHECK VALUE
32			
42			
52			
62			
72			
82			
92			
102			
112			

VDFG	USE	OUTPUT VARIABLE	CHECK VALUE
37			
47			
57			
67			
77			
87			
97			
107			
117			

MULT	USE	MULT	USE	MULT	USE	MULT	USE	FDFG	TYPE	USE	FDFG	TYPE	USE	FDFG	TYPE	USE
3		33		63		93		32			62			92		
8		38		68		98		37			67			97		
13		43		73		103		42			72			102		
18		48		78		108		47			77			107		
23		53		83		113		52			82			112		
28		58		88		118		57			87			117		

Figure A2.5. Nonlinear Component Assignment Sheet (Multipliers, DFG's, Limiters, and Hand Set Pots)

EAI 680 LOGIC ASSIGNMENT SHEET

PROBLEM_____ PROJECT #_____

PROGRAMMER_____ CONSOLE_____ DATE_____

F/F	OUTPUT	ENABLE	F/F	OUTPUT	ENABLE	F/F	OUTPUT	ENABLE
0A			1A			2A		
0B			1B			2B		
0C			1C			2C		
0D			1D			2D		
3A			4A			5A		
3B			4B			5B		
3C			4C			5C		
3D			4D			5D		

GATE	OUTPUT	GATE	OUTPUT	GATE	OUTPUT	GATE	OUTPUT	GATE	OUTPUT	GATE	OUTPUT
0A		0D		1A		1D		2A		2D	
0B		0E		1B		1E		2B		2E	
0C		0F		1C		1F		2C		2F	
3A		3D		4A		4D		5A		5D	
3B		3E		4B		4E		5B		5E	
3C		3F		4C		4F		5C		5F	

MONO	FUNCTION	SETTING	DIFF	FUNCTION	PB	FUNCTION
00			00		0	
01			01		1	
02			02		2	
40			40		3	
41			41		4	
42			42		5	

COUNTER	FUNCTION	TW	U/D
1			
3			
5			

INTERVAL	FUNCTION	SETTING
A		
B		
C		

Figure A2.6. Logic Assignment Sheet

EAI 680 INTERFACE ASSIGNMENT SHEET

PROBLEM_____ PROJECT#_____

PROGRAMMER_____ CONSOLE_____ DATE_____

TRAY	COMPARATOR OUTPUT	LATCH	D/A SWITCH INPUT	RELAY "+" STATE
4				
9				
14				
19				
24				
29				
34				
39				
44				
49				
54				
59				
64				
69				
74				
79				
84				
89				
94				
99				
104				
109				
114				
119				

Figure A2.7. Interface Assignment Sheet

In addition to labeling the output, space is provided in the flip-flop area to indicate the enable input, if used. Note that the "A" flip-flop may be enabled independently and the other three may be enabled in a group (see Paragraph 15.3.3).

All six monostables, differentiators, and pushbuttons are listed. For the monostable timers, space is provided for the numerical setting. For counters, space is provided for the two-digit thumbwheel (TW) setting, and an indication of the direction of the count (Up or Down).

APPENDIX 3

STARTUP PROCEDURE

3.1 APPLYING POWER

Assuming the computer is properly installed and appropriate power connections have been made, the machine may be turned on simply by depressing the "POWER ON" switch on the analog readout panel. When the power comes on, there will be overloads initially, but these should go away in about 10 - 20 seconds if the computer is put in the *PC* mode. After applying power, the operator should check the indicators on the control panel. It is recommended that they be put in the following mode during warmup:

1. *Analog Mode* - PC
2. *Logic Mode* - CLEAR
3. *Signal Selector* - CLEAR, then address a pot, then GO.
4. *Pot Address Control* (On analog readout panel) - KEYBOARD position.

3.2 INSERTING THE PATCH PANEL

The patch panel is motor-driven, and hence can only be inserted with the power on. An interlock prevents removal of the patch panel in any mode except *SP* or *PC*.

To insert the panel, hold it in both hands and squeeze the spring-loaded levers in the handles. Insert the panel straight - do not "pivot" it in. Once it is in, release the levers in the handles. The panel should now be latched in place securely, but the patchcords will not make electrical contact with the terminals in the patch bay until the drive motor is engaged. Depress the "PATCH PANEL ENGAGE" button on the analog readout panel, and hold it in. When the patch panel is engaged, this button will light.

The computer is now ready for use. However, to obtain maximum accuracy from the computer, a 20-minute warmup period is recommended before setting pots or making runs.

APPENDIX 4

USES OF THE LOG/EXPONENTIAL DFG

This appendix lists several typical applications of the log/exponential DFG, including scaling information. The circuits are presented in general form, with computer variables as inputs and outputs. The computer variables will range between 0 and 1 in magnitude, and are denoted by the letters X, Y, and Z. In most cases, the general circuit is illustrated with a specific example to show the relation between computer variables and problem variables. The letters P and Q are used for problem variables; if a *problem* variable P has a maximum of 25 pounds/square inch, then the corresponding *computer* variable is (P/25).

Input "gains" are shown in many of these diagrams. In most cases, the "gains" will be of the order of magnitude of 10 or 20. An input "gain" in one of these circuits is merely a shorthand notation for an input resistor, following the convention that a gain 1 resistor is 100K. The input resistor value is inversely proportional to the gain; thus a "Gain 10" resistor means a 10K input, and a "Gain 100" resistor means a 1K input. This convention is followed in the labeling of the input resistors on all summers and combination amplifiers, and on all uncommitted resistors. Networks of "Gain 10" and "Gain 1" resistors appear at the top of all DFG trays and multiplier trays respectively. There is a "Gain 100" resistor (1K) in each log/exponential tray; this resistor is useful in generating wide-range exponentials. Note that gains greater than 10 may be obtained by combining resistors in parallel; two gains of 10 in parallel provide a gain of 20, for example.

NOTE

It is generally convenient to use the log/exponential DFG with the Junction Inverter in the same tray. When doing so, it should be kept in mind that this amplifier does not follow the resistor convention mentioned in the preceding paragraph. The input and feedback resistors are 10K each. These are desirable values to use with this amplifier, since the log/exponential DFG is designed for use with 10K resistors. However, from the point of view of patching, it must be remembered that the input terminal marked "1" is actually a "gain 10" resistor.

For every circuit illustrated on the following pages, there is a dual circuit obtained by:

1. Changing all +DFG's to -DFG's.
2. Changing signs on all inputs and outputs (including reference voltage).
3. Reversing externally patched diodes, if any.
4. Changing "-LIM" to "+LIM" and vice versa on limited summers and JI's.

The use of dual circuits effectively doubles the number of examples given. An illustration of the dual principle is given in Paragraph 4.11.

Except as noted, all logs are natural (base e) logs. To assist in programming, scaling, and checkout, a short table of natural logs and exponentials is given at the end of this appendix.

4.1 BASIC EXPONENTIAL CIRCUIT

4.1.1 General Case

The basic exponential (inverse log) circuit is given in Figure A4.1. Note that the "Gain 10" input means a 10K resistor; the easiest way to get this is to use the "HG" terminal for the input, which also disconnects the feedback resistor.

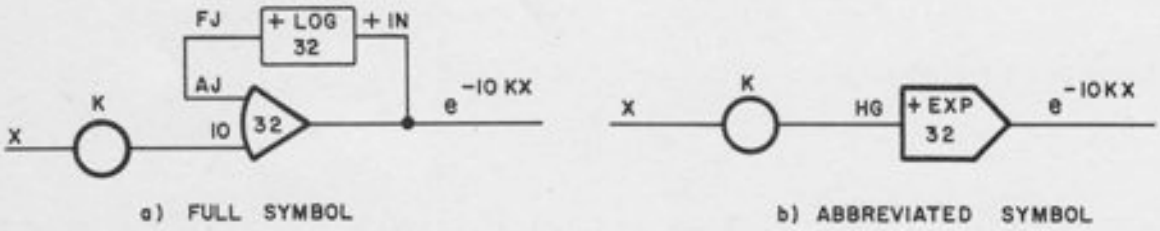


Figure A4.1. Basic Exponential Circuit

4.1.2 Scaled Example

Suppose we want to generate e^{-KP}, where $0 \leq P \leq 20$, and $K \cong 0.3$. The scaled input is (P/20), and the desired scaled output is $\left[e^{-KP}\right]$. The scaled equation is

$$\left[e^{-KP}\right] = e^{-10(2K) \cdot (P/20)}$$

Note that the product of the input (P/20), the pot-setting (2K) and the input "gain" (10) gives KP. The factor of 2 in the pot-setting is necessary to keep the equation in balance.

4.2 WIDE-RANGE EXPONENTIAL

4.2.1 General

As explained in Chapter 9, the log/exponential generator is designed to produce an exponential output with a range of e^{10}, or about 20,000 to 1. If the problem variable exceeds this range, the calculated pot-setting will turn out to be greater than unity. In this case, two additional steps must be taken:

1. Additional input resistors must be patched in parallel to increase the gain.
2. A +LIMIT connection (see Paragraph 9.1.3) must be patched to prevent the output from becoming negative for large inputs. This is necessary because when the design range of the DFG is exceeded, (i.e., when the input passes the last breakpoint) the output decreases linearly, rather than exponentially. The limit assures that the output remains zero instead of "crossing over" and becoming negative.

4.2.2 Scaled Example

Given: $0 \leq P \leq 50$, $K = 0.3$

Problem: To generate $\left[e^{-KP}\right]$ from the scaled input (P/50)

Solution: Since $K \cdot P\ (MAX) = 15$, the range of the required exponential is greater than that of the DFG. This indicates that additional gain is necessary.

Developing the scaled equation, as in the previous example:

$$\left[e^{-KP}\right] = e^{-10(5K) \cdot (P/50)}$$

where the factor of 10 represents the standard "Gain 10" resistor. Since the factor in parenthesis (5K) is greater than unity, it is not an achievable pot-setting. Re-writing the equation, using a gain of 20, we obtain:

$$\left[e^{-KP}\right] = e^{-20 \cdot (2.5K) \cdot (P/50)}$$

The circuit diagram is given in Figure A4.2. The "Gain 20" input may be easily obtained by connecting the pot to *both* the "1" input (really a "10" input for this purpose) and the "HG" input. The two gains of 10 in parallel provide the necessary gain of 20. If gains larger than 20

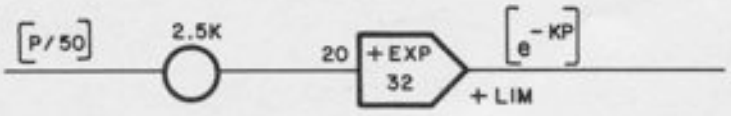


Figure A4.2. Circuit Diagram for Scaled Example

are necessary, then additional "gain 10" resistors may be added, or the "gain 100" resistor may be used. In this case, a pin must be used to remove the regular feedback resistor from amplifier 32. Note also the "+LIM" connection, which limits the output to positive values and hence prevents zero crossover.

4.3 EXPONENTIAL WITH ARBITRARY SCALE FACTOR

4.3.1 General

The exponential function e^{-KX} has its maximum value when the input X is at its minimum. If the minimum value of X is zero, then the maximum value of the exponential is unity, and $\left[e^{-KX}\right]$ is a properly scaled analog variable. This scaling for the exponential was assumed in all previous examples.

However, if the minimum value of X is not zero, then the maximum value of the exponential is not unity, and an arbitrary scale factor must be included. The general circuit is given in Figure A4.3. Note that the sign of the reference bias depends on the magnitude of A. The output of the pot is -(1/10) log A, which is negative if $A > 1$ and positive if $A < 1$.

4.3.2 Scaled Example

Given: $10 \leq P \leq 25$; $K = 0.6$

Problem: To generate e^{-KP}, given the scaled input (P/25).

Solution: The maximum value of the exponential is $e^{-6} = 1/400$. Hence, we should choose A = 400, and generate the scaled exponential $\left[400\ e^{-KP}\right]$. The setting on the bias pot becomes (log 400)/10 = .5591.

In this case, the minimum value of the output is $400 \cdot e^{-15}$, which is $> 1/20,000$. Hence, no LIMIT connection is necessary.

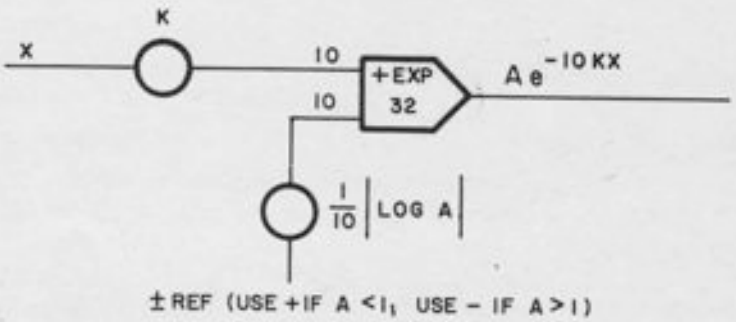


Figure A4.3. Exponential with Arbitrary Scale Factor

Another method of handling the case where the minimum value of the input is not zero is to generate an auxiliary variable whose minimum *is* zero. In this case, the variable would be $\Delta P = P - 10$.

4.4 GENERATING FRACTIONAL POWERS

4.4.1 General

The general N-th power is illustrated in Figure A4.4. Note that in both cases, +log DFG's are used. The "gain 10" input on DFG 37 may be most conveniently obtained by using the "HG" input. As shown, the circuit is restricted to values of $N \leq 1$, since N appears as a pot-setting. Larger exponents may be accommodated by using more gain; e.g., a setting of N/2 and a gain of 20, or a setting of N/3 and a gain of 30, etc. Gains beyond 20 require additional input resistors. For very large gains (a rare occurrence) the "Gain 100" resistor may be used.

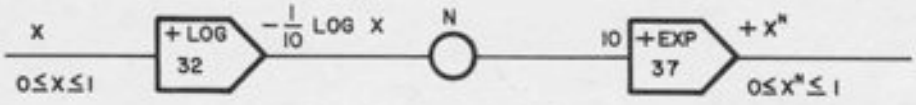


Figure A4.4. Generating Nth Power

For $N < 1$, no +LIMIT connection is necessary on amplifier 37. For $N > 1$, the limit connection is usually necessary for amplifier 37, since X^N covers a wider range than X itself. For example, if X has a minimum value of 10^{-3} (0.1% of its maximum value) then X^2 has a minimum of 10^{-6}, which is outside the range of the DFG, even if X itself is not.

In the case $N \geq 1$, the output will be correct for X = 0 (it will be zero). The +LIM connection on the output amplifier assures this, even though the DFG itself is driven outside its design range.

4.4.2 Scaled Example

Given: $0 \leq P \leq 25$

Problem: To generate an output proportional to $P^{1.4}$ given the scaled input (P/25).

Solution: Use the above circuit with N = 1.4, and (P/25) as input. The output will be $(P/25)^{1.4}$ which is properly scaled. Note the scale factor for the output.

If the output is written as $K \cdot P^N$, where K is the output scale factor, then $K = (1/25)^N$. Thus the value of the output scale factor depends upon the value of the exponent N. This dependence is necessary to insure that the magnitude scaling of the output is correct for any value of N; that is, that a properly scaled input produces a properly scaled output.

4.5 MULTIPLICATION WITH BUILT-IN SCALE FACTOR

4.5.1 Minimum Amplifier Circuit

Two positive signals may be multiplied together with only *one* amplifier and three DFG's (two "plus" and one "minus"). The circuit is given in Figure A4.5. Note the -LIM connection on the output amplifier; this is almost always necessary, since the output covers a wider range than either factor (e.g., when $x = y = 10^{-3}$, $xy = 10^{-6}$).

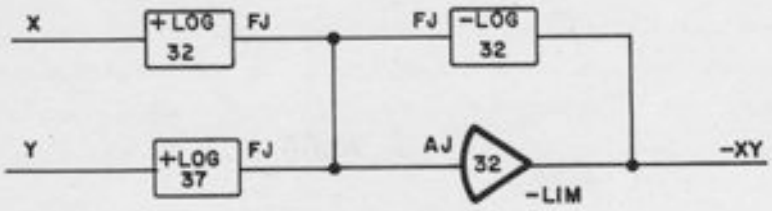


Figure A4.5. Multiplication - Single Amplifier

4.5.2 Many Common Factors

If many products occur with the same factor, then circuit of Figure A4.5 is generally not the most economical, even though it uses the fewest amplifiers. To avoid generating the log of a factor more than once, it is preferable to use an output amplifier for the logarithm, so that the log is then available for "fanning out" to more than one product. See Figure A4.6. Although

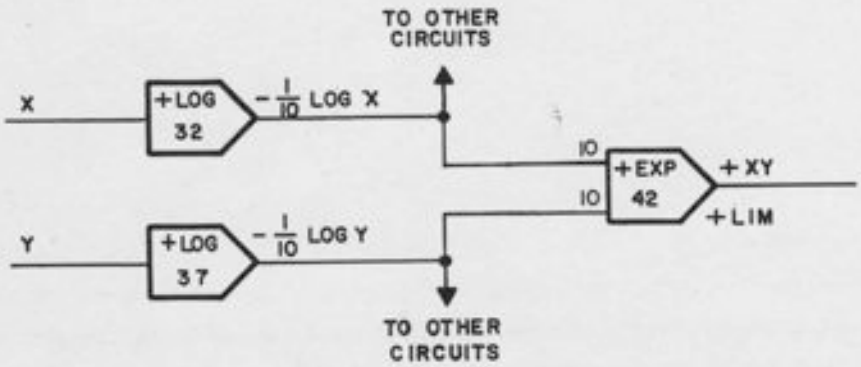


Figure A4.6. Multiplication - Many Products with Common Factors

this circuit uses more amplifiers than the one above, it uses fewer DFG's if one or more factors are common to the same product. In problems with many interrelated products, this circuit is the most economical. The equipment requirement is one amplifier and one DFG per *factor* and one amplifier and one DFG per *product*.

4.6 MULTIPLICATION WITH ARBITRARY SCALE FACTOR

4.6.1 General

The multiplication circuit in Figure A4.5 has a "built-in" scale factor similar to that on other multipliers, such as the quarter-square multiplier. If both scaled inputs are at their respective maximum values simultaneously (i.e., 1.0 unit) then the output will also be at its maximum (1.0 unit).

This built-in scale factor is generally a good one to use, but it is poor if the inputs do not reach their respective maximum values simultaneously. In case the maximum value of the product is known to be less than the product of the maximum values of the factors, a better (and more accurate) scaling is possible. The general circuit is given in Figure A4.7.

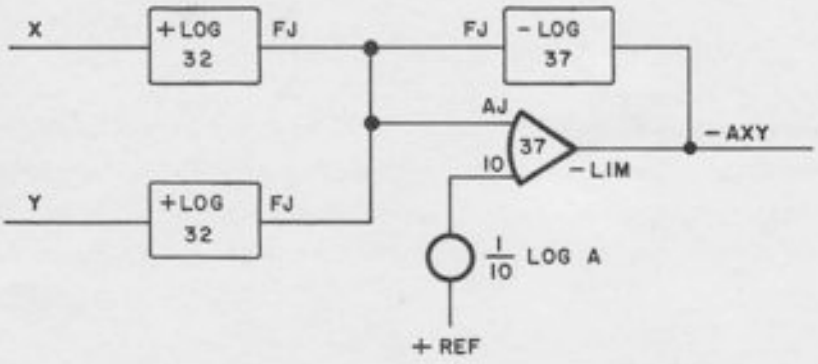


Figure A4.7. Multiplication with Arbitrary Scale Factor

Note that we always have A ≥ 1. This is because the "built-in" scale factor is always either correct (in case the maximum inputs occur simultaneously) or else too small (in case one input is small when the other is large). Hence, it may prove desirable to increase the output (relative to the "built-in" scale factor) but never to decrease it.

4.6.2 Scaled Example

Given: $0 \leq P \leq 20$, $0 \leq Q \leq 5$

$0 \leq PQ \leq 50$

Problem: To generate (PQ/50), given the scaled inputs (P/20) and (Q/5).

Solution: Straight-forward multiplication of (P/20) by (Q/5) would give (PQ/100), which would be proper scaling if the variables "peaked" simultaneously, so that the maximum was actually 100. However, we are assuming that they do not "peak" simultaneously, and that the maximum value of the product is estimated as 50. Since we want to amplify the output by a factor of 2, we should choose A = 2 in the general circuit. The pot-setting is then 1/10 (log 2) = 0.06932.

Since this is < 0.1, we may improve the accuracy by using a "gain 1" (100K) resistor and a setting of 0.6932. If this is done, the "gain 1" resistor must be externally patched, since the "1" input on a Junction Inverter, as explained above, is really a "gain 10" (10K) resistor. Also, if the "HG" terminal is not used as an input, a pin must be inserted to remove the feedback resistor.

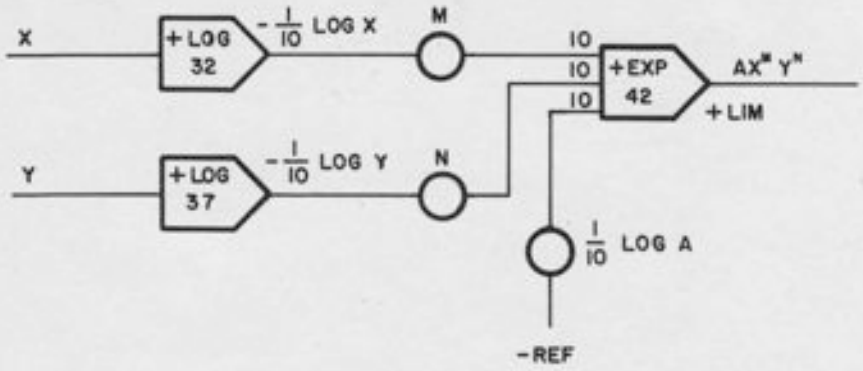


Figure A4.8. Products of Powers

4.7 PRODUCTS OF POWERS

In many applications (for example, in chemical kinetics problems) it is necessary to generate terms such as $X^M Y^N$, where X and Y are variables and M and N are positive constants (which need not be integers). Such outputs may be generated by the circuit of Figure A4.8. An arbitrary scale factor is included for the output in case X and Y do not "peak" simultaneously. This circuit may be easily generalized to handle products with more than two factors. As shown, the circuit is restricted to exponents ≤ 1.0; however, larger exponents may be handled by using larger gains.

4.8 DIVISION

4.8.1 General

The general division circuit is shown in Figure A4.9. Note the following facts:

1. The +LIM connection may or may not be necessary, depending on the expected minimum value of the quotient.

2. The factor A is chosen to scale the quotient properly, and will always be ≥ 1. To see this, assume that both X and Y have maximum values of unity (which will be true if they are properly scaled computer variables). Then the maximum value of the quotient is *at least* unity (for example, when $y = 1.0$, the quotient $y/x \geq 1.0$) and may be much larger (e.g., if x is small when y is large). Hence, it may prove necessary to *attenuate* the output by means of the bias pot, but it will never be necessary to *amplify* it.

3. This circuit works only in one quadrant; we must have ($0 \leq x \leq 1$ and $0 \leq y \leq 1$). (Note that this means that the input voltage to the -LOG DFG must be *negative* since the input is -y.) The output quotient will be positive.

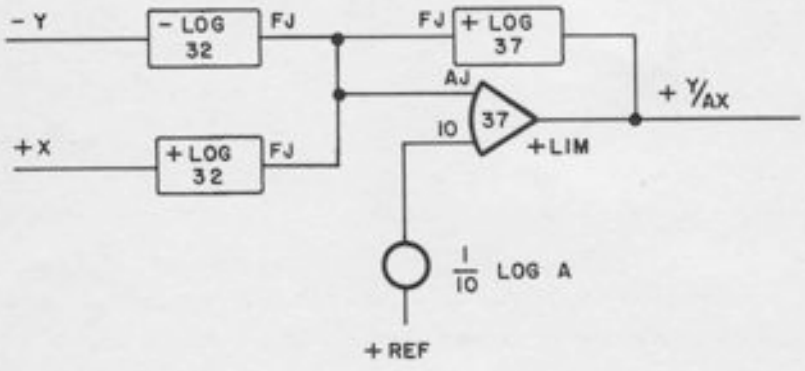


Figure A4.9. Division

4.8.2 Scaled Example

Given: $0 \leq P \leq 500$, $0 \leq Q \leq 100$ and $0 \leq P/Q \leq 20$.

Problem: To generate the scaled output (P/20Q) from the scaled inputs (P/500) and (Q/100).

Solution: Dividing the scaled numerator by the scaled denominator, we obtain (P/500) $\div$ (Q/100) = P/5Q. The desired scaled output is P/20Q, which is one-fourth of this. Hence we choose A = 4. The scaled equation becomes:

$$\frac{P}{20Q} = \frac{(P/500)}{4(Q/100)}$$

which is in the proper format (Y/AX) for the general circuit given above. The pot-setting is $\frac{1}{10}$ log 4 = 0.1386.

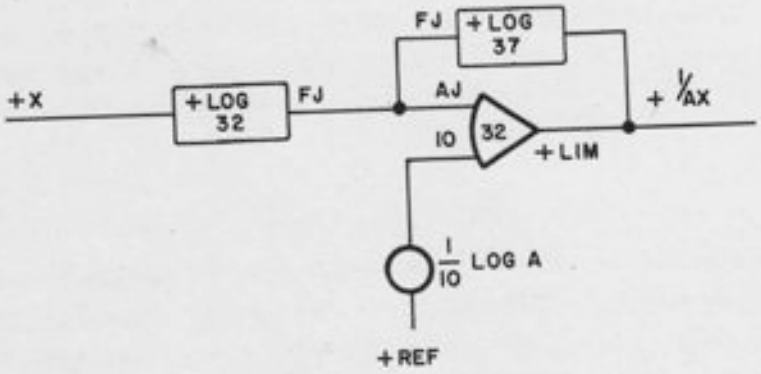


Figure A4.10. Reciprocal Generation

4.9 RECIPROCALS

4.9.1 General

The general circuit for producing the reciprocal of a given variable is given in Figure A4.10. It may be considered as a division circuit with a constant numerator; hence, it uses one less log/exponential DFG than the standard division circuit. The following points should be noted:

1. The factor A > 1 should be determined by the maximum expected value of 1/x, which corresponds to the *minimum* value of x.

2. If the ratio of the maximum value of the input to its minimum value is $\leq e^{10}$ (about 20,000), then the calculated setting on the bias pot will be ≤ 1.0. In this case, no +LIM connection is required to prevent zero crossover.

3. If the range of the input is greater than 20,000 to 1, the bias pot will have to be connected to a larger gain. A +LIM connection will then be necessary to prevent zero crossover.

4.9.2 Scaled Example

Given a problem variable Q, $20 \leq Q \leq 1000$. It is required to generate a properly-scaled reciprocal. Solution: Since the maximum value of 1/Q occurs when Q = 20, we should scale the reciprocal as (20/Q). The input Q is, of course, scaled as (Q/1000). The scaled equation may be written as

$$(20/Q) = \frac{1}{A(Q/1000)}$$

which expresses the desired relation between the scaled input (Q/1000) and the scaled output (20/Q). The factor A must be chosen to balance the equation, solving for A we see that A = 50. The pot-setting then becomes $\frac{1}{10}$ Log A = .3912, using the table of natural logs given in this appendix.

4.10 BASE 10 LOGS

In case a base 10 logarithm is desired, it may be obtained from the base e logarithm by multiplying by the appropriate conversion factor. This may be most easily accomplished by means of a pot in the feedback of a high-gain amplifier. If 4-decade scaling is desired, the appropriate equation is:

$$(1/4 \log_{10} x) = (1/10 \log_e x)/0.4 \log_e 10$$

The circuit diagram is given in Figure A4.11. Note that this is the regular "base e" log circuit, except for the use of pot feedback, which divides the output by the pot-setting $0.4 \log_e 10 = 0.9210$.

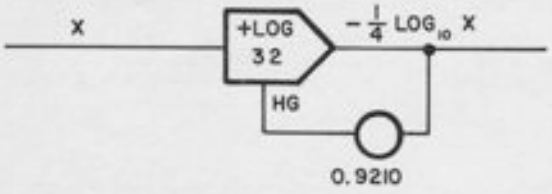


Figure A4.11. Base 10 Log

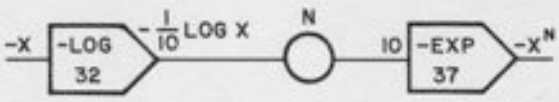


Figure A4.12. Illustration of a Dual Circuit

4.11 ILLUSTRATION OF A DUAL CIRCUIT

The rules for obtaining a dual circuit are given at the beginning of this appendix. As an example, Figure A4.12 is the dual circuit of Figure A4.4.

Note that a given circuit and its dual perform "essentially" the same function, except for sign. Choice between the two in a given case will depend upon the following considerations:

1. Sign. What signs of the inputs are available, and what sign of the output is desired? Which circuit uses fewer external inverters?

2. Available DFG's. How many DFG's of each type are available? Note that if a circuit uses more "plus" than "minus" DFG's, the opposite will be true for its dual.

4.12 LOG/EXPONENTIAL TABLES

The following short tables may prove helpful in programming, scaling, and checking problems using the log/exponential DFG. Values not in this table may be calculated using known properties of the log function - e.g., log (150) = log (75) + log (2); log (1.25) = log (5/4) = log 5 - log 4.

Natural Logs

X	Log X	X	Log X	X	Log X	X	Log X	X	Log X
1	0.00000	21	3.04452	41	3.71357	61	4.11087	81	4.39445
2	0.69315	22	3.09104	42	3.73767	62	4.12713	82	4.40672
3	1.09861	23	3.13549	43	3.76120	63	4.14313	83	4.41884
4	1.38629	24	3.17805	44	3.78419	64	4.15888	84	4.43082
5	1.60944	25	3.21888	45	3.80666	65	4.17439	85	4.44265
6	1.79176	26	3.25810	46	3.82864	66	4.18965	86	4.45435
7	1.94591	27	3.29584	47	3.85015	67	4.20469	87	4.46591
8	2.07944	28	3.33220	48	3.87120	68	4.21951	88	4.47734
9	2.19722	29	3.36730	49	3.89182	69	4.23411	89	4.48864
10	2.30259	30	3.40120	50	3.91202	70	4.24850	90	4.49981
11	2.39790	31	3.43399	51	3.93183	71	4.26268	91	4.51086
12	2.48491	32	3.46574	52	3.95124	72	4.27667	92	4.52179
13	2.56495	33	3.49561	53	3.97029	73	4.29046	93	4.53260
14	2.63906	34	3.52636	54	3.98898	74	4.30407	94	4.54329
15	2.70805	35	3.55535	55	4.00733	75	4.31749	95	4.55388
16	2.77259	36	3.58352	56	4.02535	76	4.33073	96	4.56435
17	2.83321	37	3.61092	57	4.04305	77	4.34381	97	4.57471
18	2.89037	38	3.63759	58	4.06044	78	4.35671	98	4.58497
19	2.94444	39	3.66356	59	4.07754	79	4.36945	99	4.59512
20	2.99573	40	3.68888	60	4.09434	80	4.38203	100	4.60517

Exponential Function

X	e^{-X}	X	e^{-X}	X	e^{-X}	X	e^{-X}	X	e^{-X}
0.0	1.000000	2.0	0.135335	4.0	0.018316	6.0	0.0024788	8.0	0.0003355
0.1	0.904837	2.1	0.122456	4.1	0.016573	6.1	0.0022429	8.1	0.0003035
0.2	0.818731	2.2	0.110803	4.2	0.014996	6.2	0.0020294	8.2	0.0002747
0.3	0.740818	2.3	0.100259	4.3	0.013569	6.3	0.0018363	8.3	0.0002485
0.4	0.670320	2.4	0.090718	4.4	0.012277	6.4	0.0016616	8.4	0.0002249
0.5	0.606531	2.5	0.082085	4.5	0.011109	6.5	0.0015034	8.5	0.0002035
0.6	0.548812	2.6	0.074274	4.6	0.010052	6.6	0.0013604	8.6	0.0001841
0.7	0.496585	2.7	0.067206	4.7	0.009095	6.7	0.0012309	8.7	0.0001666
0.8	0.449329	2.8	0.060810	4.8	0.008230	6.8	0.0011138	8.8	0.0001507
0.9	0.406570	2.9	0.055023	4.9	0.007447	6.9	0.0010078	8.9	0.0001364
1.0	0.367879	3.0	0.049787	5.0	0.006738	7.0	0.0009119	9.0	0.0001234
1.1	0.332871	3.1	0.045049	5.1	0.006097	7.1	0.0008251	9.1	0.0001117
1.2	0.301194	3.2	0.040762	5.2	0.005517	7.2	0.0007466	9.2	0.0001010
1.3	0.272532	3.3	0.036883	5.3	0.004992	7.3	0.0006755	9.3	0.0000914
1.4	0.246597	3.4	0.033373	5.4	0.004517	7.4	0.0006113	9.4	0.0000827
1.5	0.223130	3.5	0.030197	5.5	0.004087	7.5	0.0005531	9.5	0.0000749
1.6	0.201897	3.6	0.027324	5.6	0.0036979	7.6	0.0005005	9.6	0.0000677
1.7	0.182684	3.7	0.024724	5.7	0.0033460	7.7	0.0004528	9.7	0.0000613
1.8	0.165299	3.8	0.022371	5.8	0.0030276	7.8	0.0004097	9.8	0.0000555
1.9	0.149569	3.9	0.020242	5.9	0.0027394	7.9	0.0003707	9.9	0.0000502
2.0	0.135335	4.0	0.018316	6.0	0.0024788	8.0	0.0003355	10.0	0.0000454

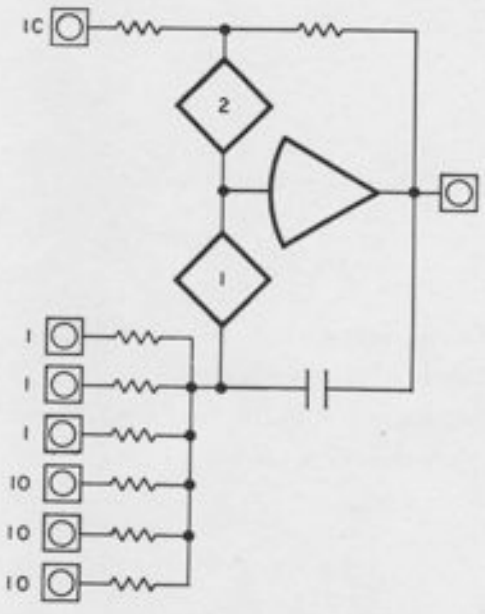
APPENDIX 5

ELECTRONIC SWITCHES

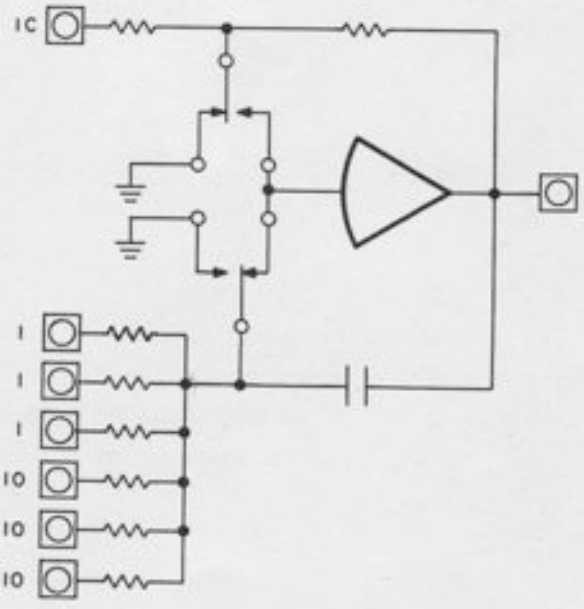
Electronic switches, or "gates" are used for mode control for integrators and track/store units. These gates are turned on and off by logic levels, and have a switching time of one microsecond or less.

These gates are represented on schematic diagrams by a diamond-shaped symbol (see, for example, Figure 6.2). The gates are used to switch input and feedback connections to the amplifier junction. In understanding the diagrams, it is important to realize that the input (and feedback) elements are shorted directly to ground whenever the gate is not conducting. In other words, each diamond-shaped symbol represents *two* electronic switches, one connecting the appropriate summing junction to ground, and the other connecting it to the amplifier junction. Thus, the summing junction is always essentially at ground potential; it is either connected directly to ground, or else to an amplifier junction (virtual ground).

This fact is important from the point of view of loading. Since most inputs to these amplifiers come from potentiometers, it is important to assure that the summing junction is at virtual ground at all times.

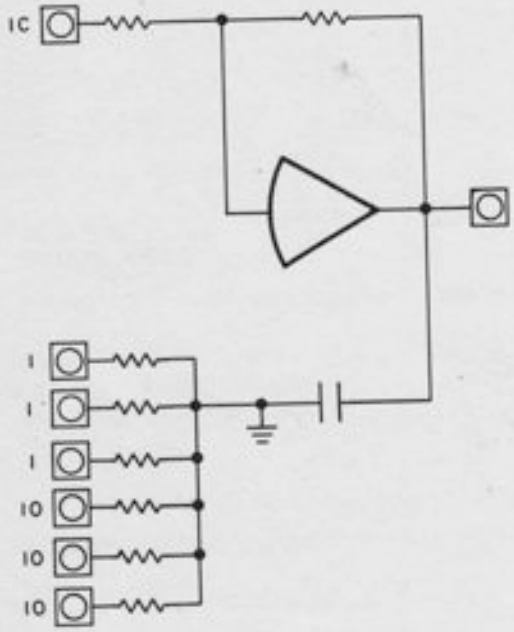


Simplified schematic for integrator. (HOLD mode circuitry omitted for clarity.)

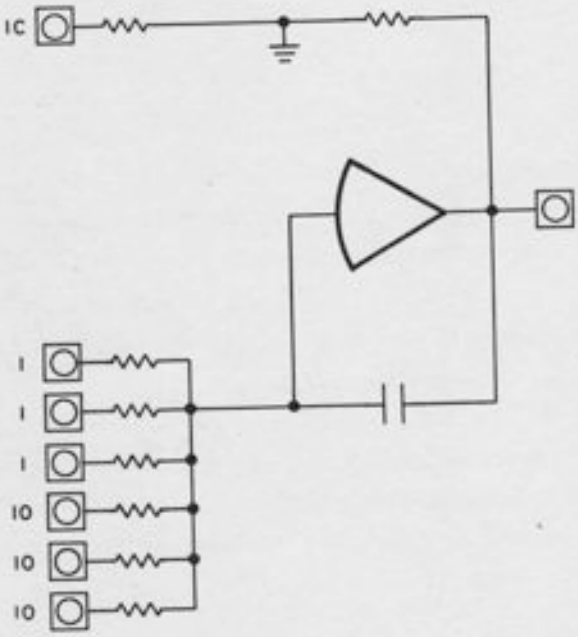


Functionally equivalent circuit, using relays.

Note that both input and feedback elements are connected to the summing junction. Hence the feedback element is also grounded when the gate is switched off. This is important for integrators and track/store units, since it assures that the feedback capacitor is charged to the appropriate amplifier voltage. For large capacitor values, a current-limiting resistor (not shown on schematic below) is used in series with the gate to prevent excessive current drain on the amplifier at high frequencies.



Effective circuit for integrator in IC mode. (Hold circuit eliminated for clarity. Note that the feedback capacitor and the input resistor are grounded.)



Effective circuit for integrator in OPERATE mode. (Note that IC summing junction is grounded.)

The D/A switch (see Paragraph 13.3) is similar to the mode control gates described above, in that it shorts the input resistor to ground when the switch is off, thus assuring proper loading at all times. However, it differs from mode control switches in that it switches only *one* input resistor, instead of several, and it does not switch the feedback element of the amplifier to which it is patched.

APPENDIX 6

NORMALLY-CLOSED PATCH PANEL SWITCHES

The 680 Computer makes extensive use of normally-closed switches behind the patch panel to reduce patching complexity. These switches make contact between various parts of a circuit internally, but allow this contact to be broken by the insertion of a patchcord.

The working of this switch is shown in Figures A6.1 to A6.3. The two points (A and B) are internal points of the circuit behind the patch panel. When nothing is patched in, points A and B are connected. When a patchcord is inserted, it makes contact with B and *breaks the connection between A and B.*

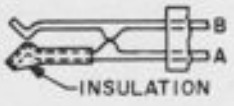


Figure A6.1. Normally-Closed Switch without Patchcord

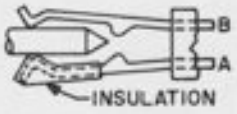


Figure A6.2. Normally-Closed Switch with Patchcord Inserted

Figure A6.3. Normally-Closed Switch as it Appears on Schematic Diagrams

Note that the symbol for the normally-closed switch consists of a large circle tangent to a small circle. The operator "patches into the large circle", and thus breaks the contact with the small circle.

This type of patch panel switch is used both for analog signals and for logic signals. As an example of its use, for logic signals, see Chapter 20. Note that if nothing is patched into the mode control terminals, the integrator operates normally (i.e., in response to the mode pushbuttons). If logic signals are patched into these terminals, the normal mode control is disconnected, and the computer is controlled by the locally patched signals.

A conventional patch panel termination is shown in Figures A6.4 to A6.6. Inserting a patchcord simply makes a single contact.

Figure A6.4. Conventional (Single) Terminal, without Patchcord

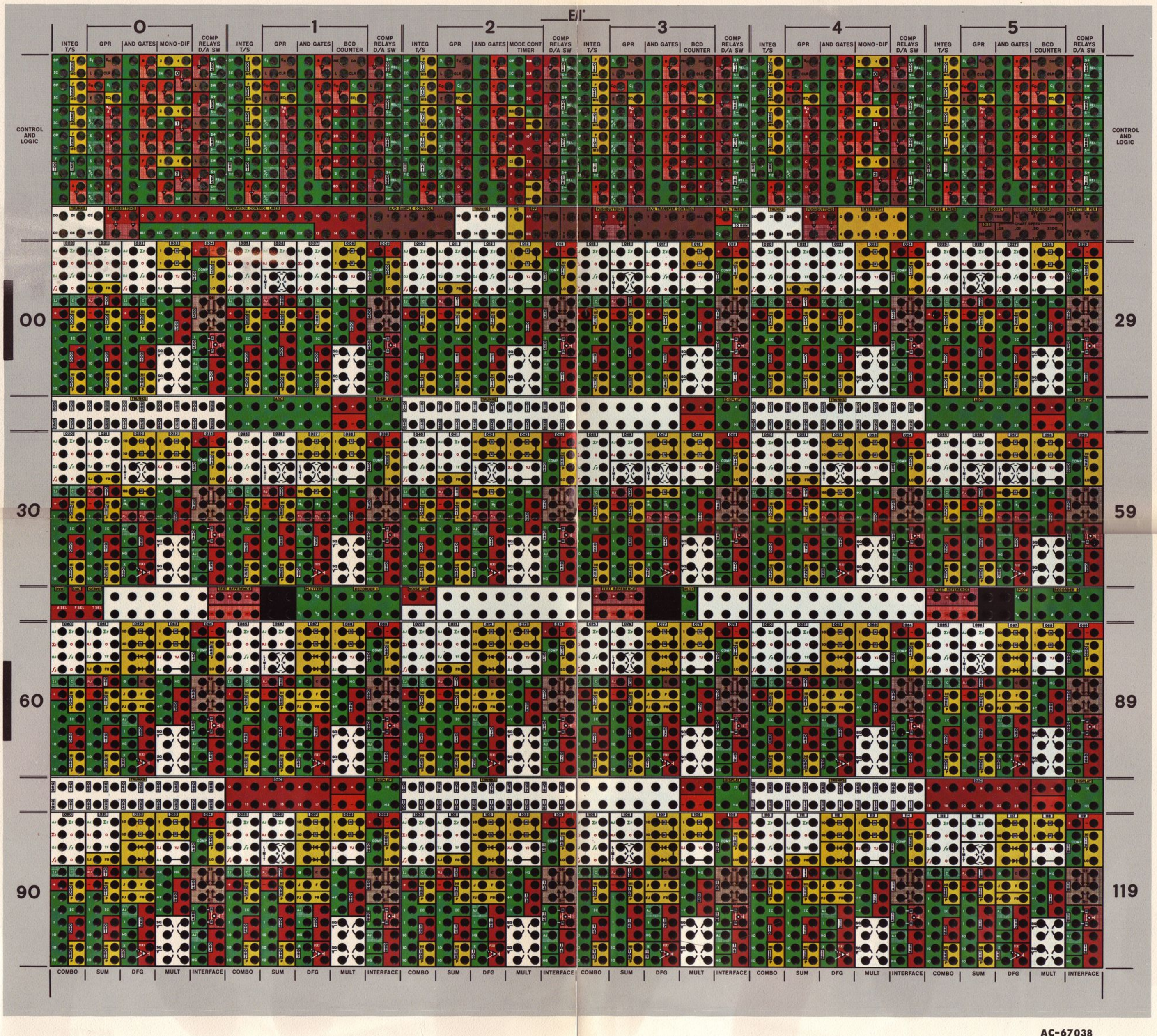
Figure A6.5. Conventional (Single) Terminal, with Patchcord

Figure A6.6. Conventional (Single) Terminal, as it Appears on Schematic Diagrams

APPENDIX 7

STANDARD 680 PATCH PANEL CONFIGURATION

The photograph in this appendix shows the standard layout of the 680 Patch Panel. The handles and latches have been removed for clarity. This illustration should be used as a guide only, since special systems may have other component configurations, particularly for multipliers and DFG's. In these cases, appropriate overlays are applied to the patch panel to indicate correct component arrangements, and the panel itself must be used as a layout guide.


E/I
0
1
2
3
4
5
INTEG T/S
GPR
AND GATES
MONO-DIF
BCD COUNTER
MODE CONT TIMER
COMP RELAYS D/A SW
CONTROL AND LOGIC
00
29
30
59
60
89
90
119
COMBO
SUM
DFG
MULT
INTERFACE

AC-67038